


# LCFC Confidential

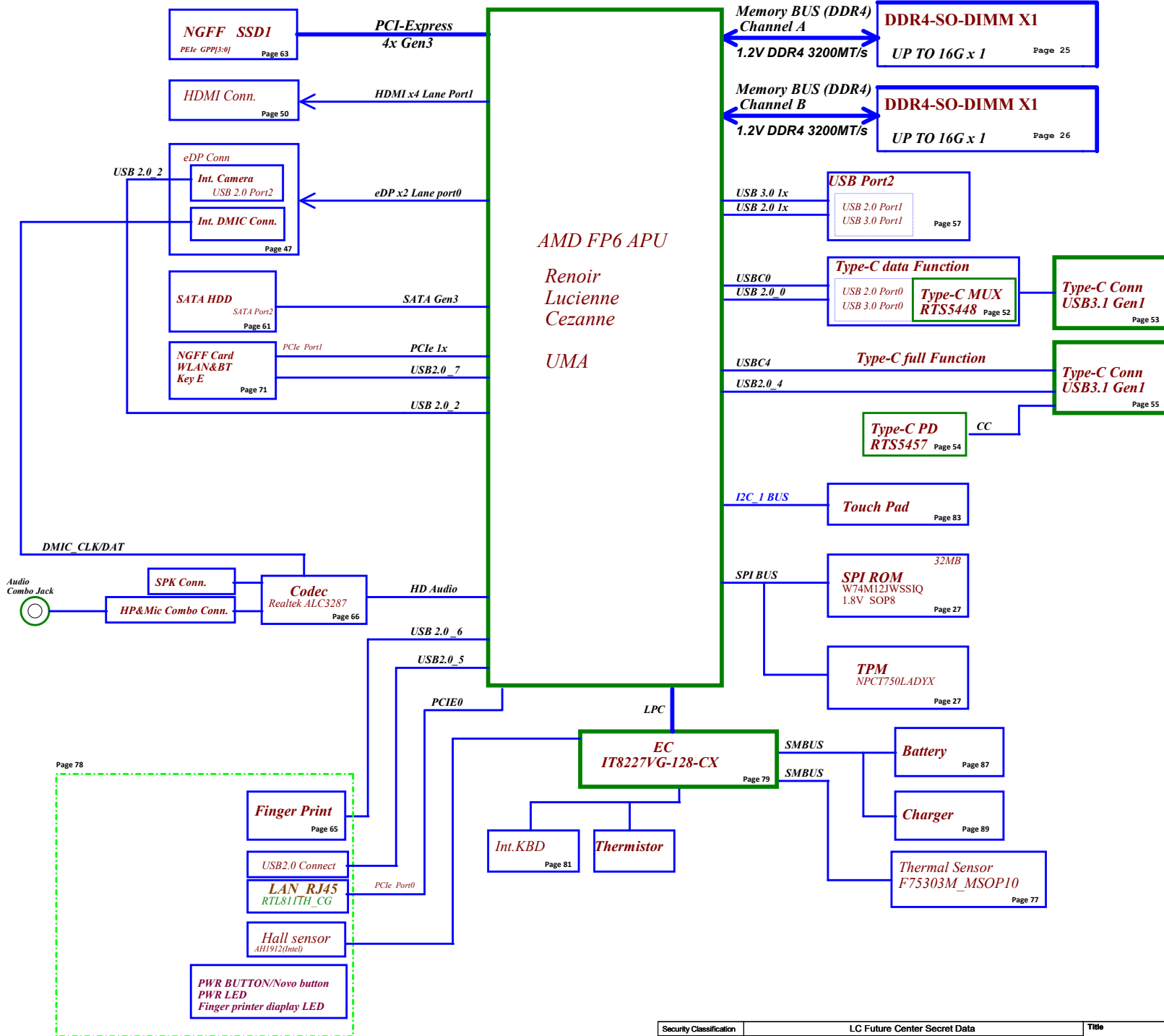
## K14 Lucienne M/B Schematics Document

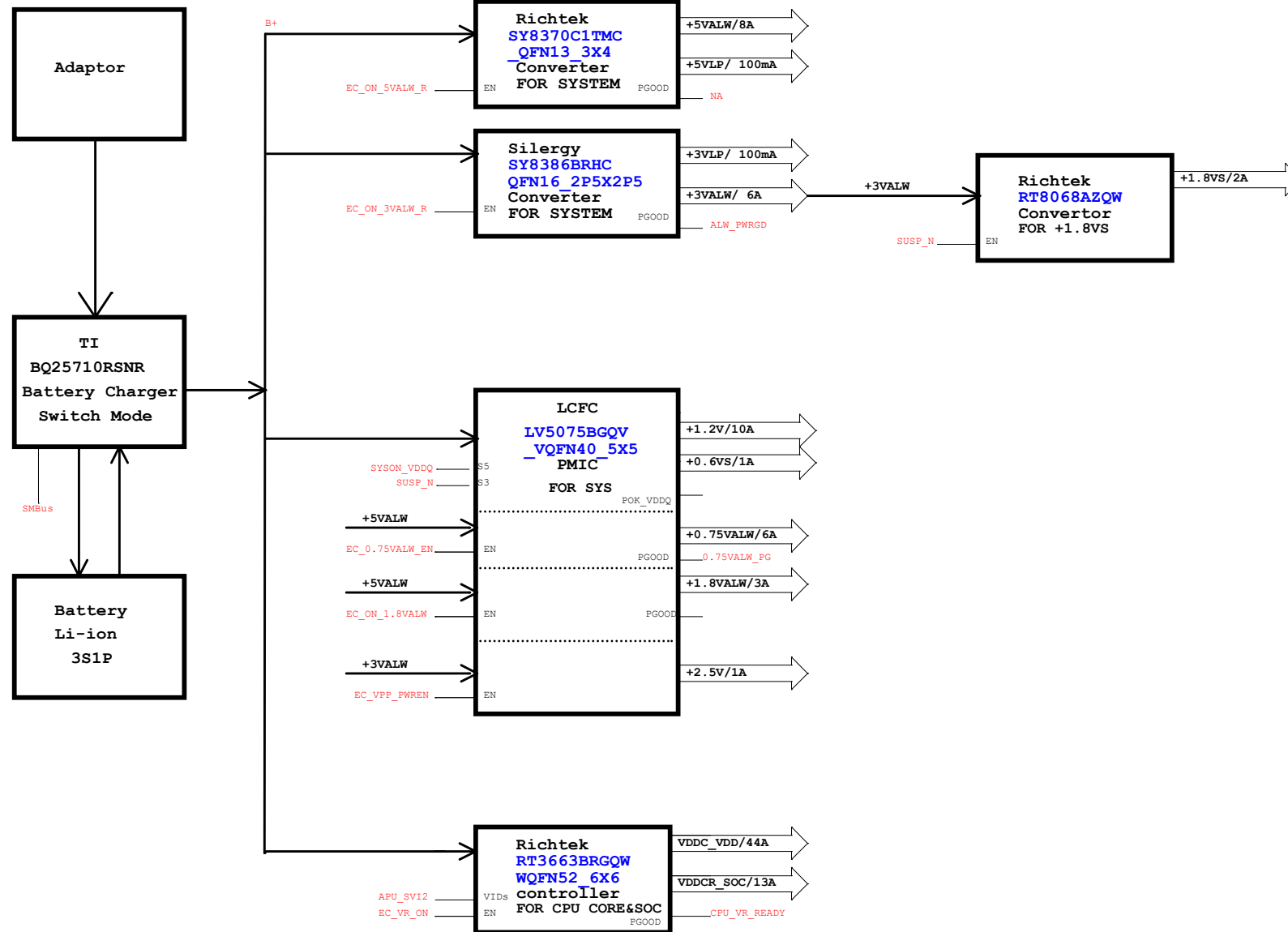
AMD FP6 Lucienne with DDR4

2021-04-21

REV:1.0

Security Classification	LC Future Center Secret Data			Title		
Issued Date	2021/09/29	Deciphered Date	2021/04/21	K14_AMD_Cezanne		
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Voltage Rails ( O --> Means ON , X --> Means OFF )

Power Plane \ State	B+ +3VL +5VL	+3VALW  +5VALW  +1.8VALW +0.75VALW		+1.2V +2.5V_DDR	+5VS +3VS +1.8VS +0.75VS +0.6VS  +VDDC_VDD +VDDCR_SOC	
S0	O	O		O	O	O
S0Ix						
S3	O	O		O	X	X
S3 Battery only	O	O		O	X	X
S5 S4 AC Only	O	O		X	X	X
S5 S4 Battery only	O	X		X	X	X
S5 S4 AC & Battery don't exist	X	X		X	X	X

HSIO Matrix

HSIO PORT		Function
USB2.0	0	Type-C USB2.0 Port 0
	1	USB3.0_F1
	2	Camera
	3	Touch_Screen Change to I2C
	4	USB2.0 Port(For DB USB2.0)
	5	Cardread
	6	FingerPrint
	7	BT
USB3.0	0	Type-C USB3.0 Port 0
	1	USB3.0_F1
	4	NC
	5	NC
DisPlay	0	eDP 2*Lane
	1	HDMI
	2	NC
	3	NC
PCIE/ SATA	PCIE0	LAN
	PCIE1	WLAN
	PCIE2/SATA0	SATA HDD
	PCIE3/SATA1	N/A
	PCIE4	N/A
	PCIE5	N/A
	PCIE6	N/A
	PCIE7	N/A
	PCIE8/SATA2	SSD
	PCIE9/SATA3	
	PCIE10	
	PCIE11	

SMBUS Control Table OK

Source \ Slave	EC IT8227C				PCH			
	EC_SMB_0 +3VS	EC_SMB_1 +3VL_EC	EC_SMB_3 +3VL_EC	EC_SMB_4 +3VL_EC	I2C0 1.8VS/3.3VS	I2C1 1.8VS/3.3VS	I2C2/SMBUS 1.8VS/3.3VS	
DGPU								
Memory Down	X	X	X	X	X	X	X	X
SODIMM							V 3VS	
BATT	X	V +3VL_EC	X	X	X	X	X	X
Charger	X	V +3VL_EC	X	X	X	X	X	X
WLAN	X	X	X	X	X	X	X	X
PMIC	X	X	V +3VL_EC	X	X	X	X	X
	X	X	X	X	X	X	X	X
Thermal Sensor	V +3VS	X	X	X	X	X	X	X
LPC&TS	X	X	X	X	V +3VS_CPU	X	X	X
TP	X	X	X	X	X	V 3VS	X	X
	X	X	X	X	X	X	X	X
	X	X	X	X	X	X	X	X

EC SMBus0 address

Device	Address
DGPU	
Thermal Sensor(NCT7718W)	
Thermal Sensor(NCT7719W)	1001_101xb
TOF	

PCH SML0 address

Device	Address
Re-Timer	TBD

PD I2C3 address

Device	Address
Re-Timer	TBD

EC SMBus1 address

Device	Address
Smart Battery	0x16
Charger	0x12

PCH SML1 address

Device	Address
PD	TBD

EC SMBus3 address

Device	Address
IMVP9	
PMIC	0x34

PCH ISH I2C0 address

Device	Address
TOF	
Accelerometer(MB)	001 1000b
Accelerometer(DB)	001 1001b
Light Sensor	1000 100xb

EC SMBus4 address

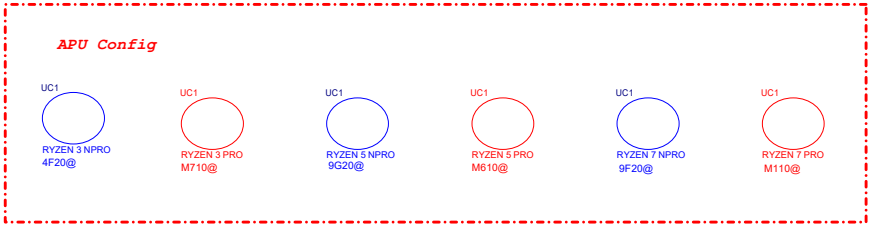
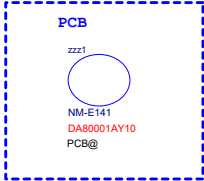
Device	Address
PD	TBD



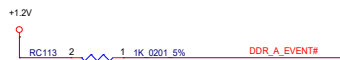
BOM Structure

BOM Structure      Description

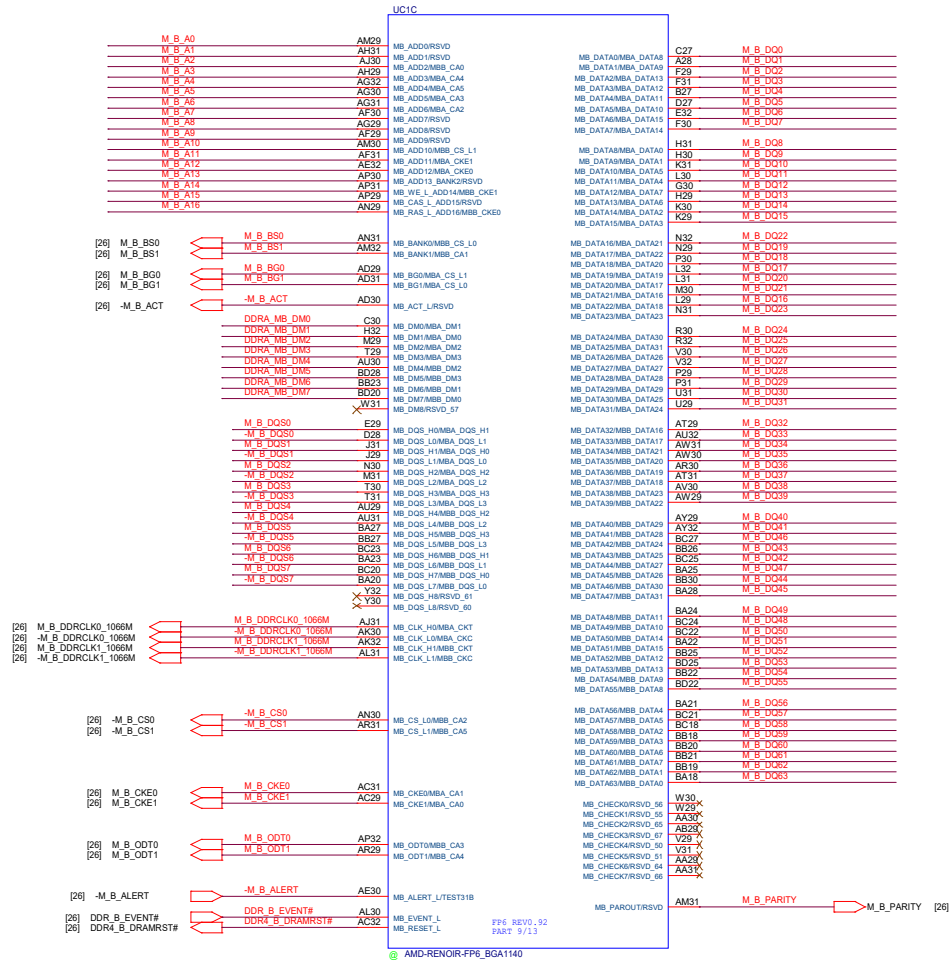
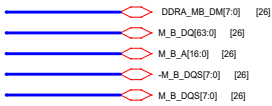
BOM config





Rev



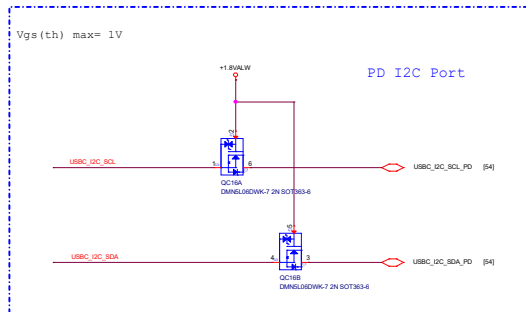
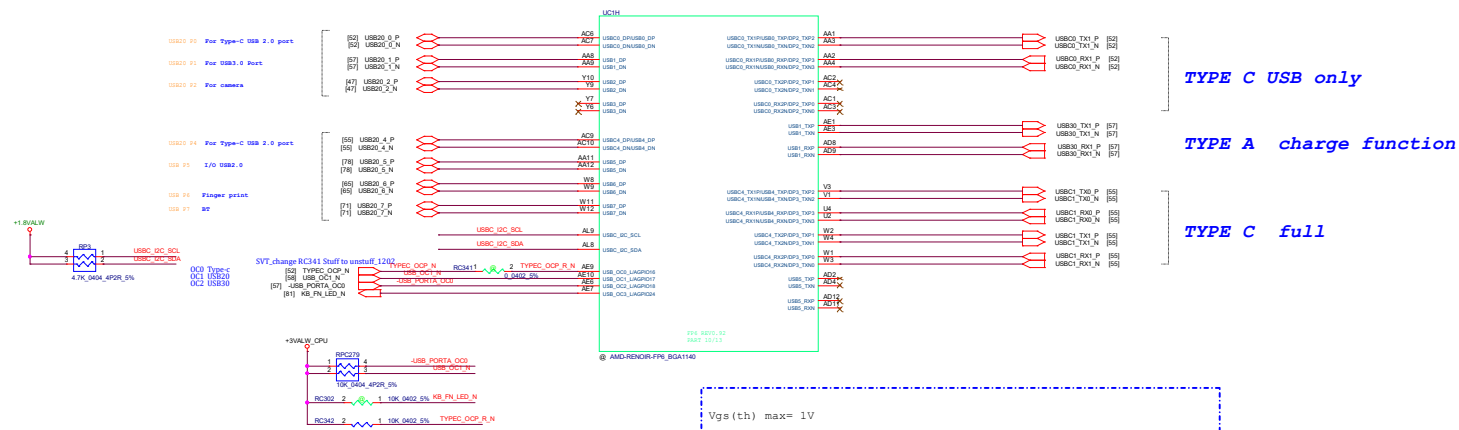
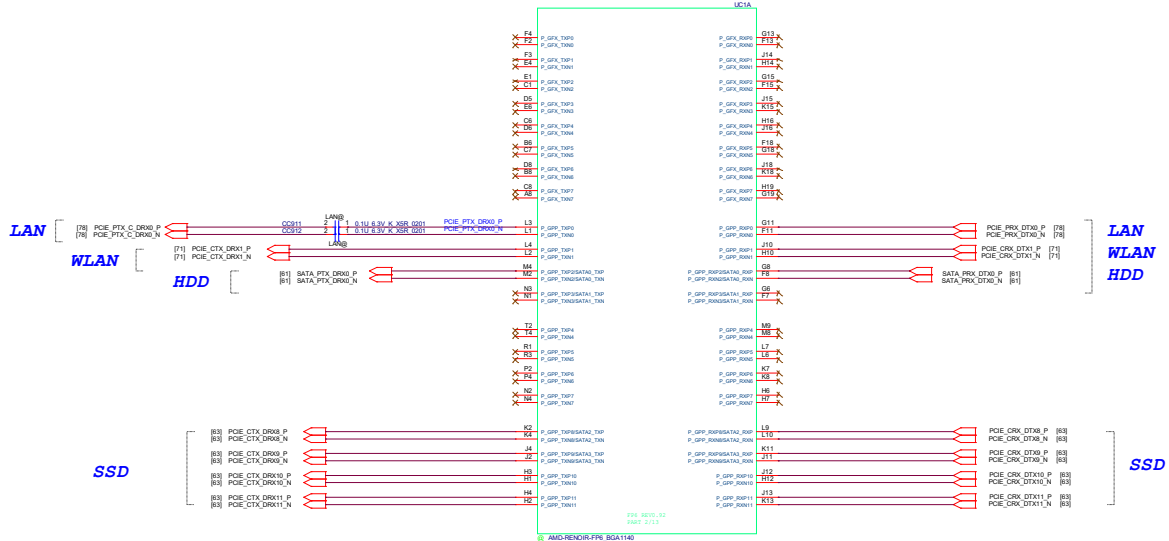




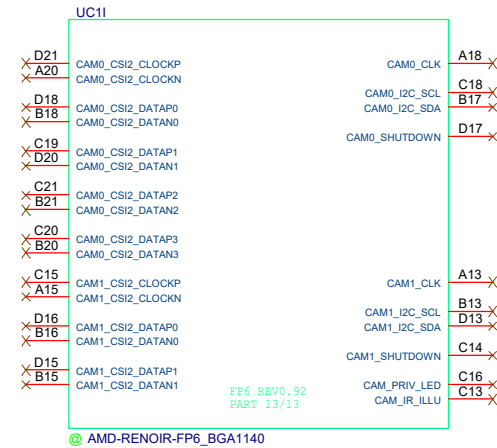
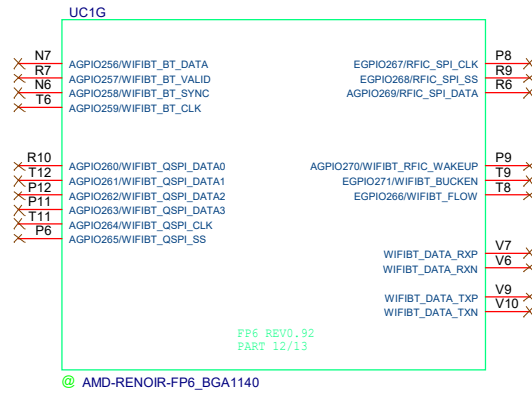






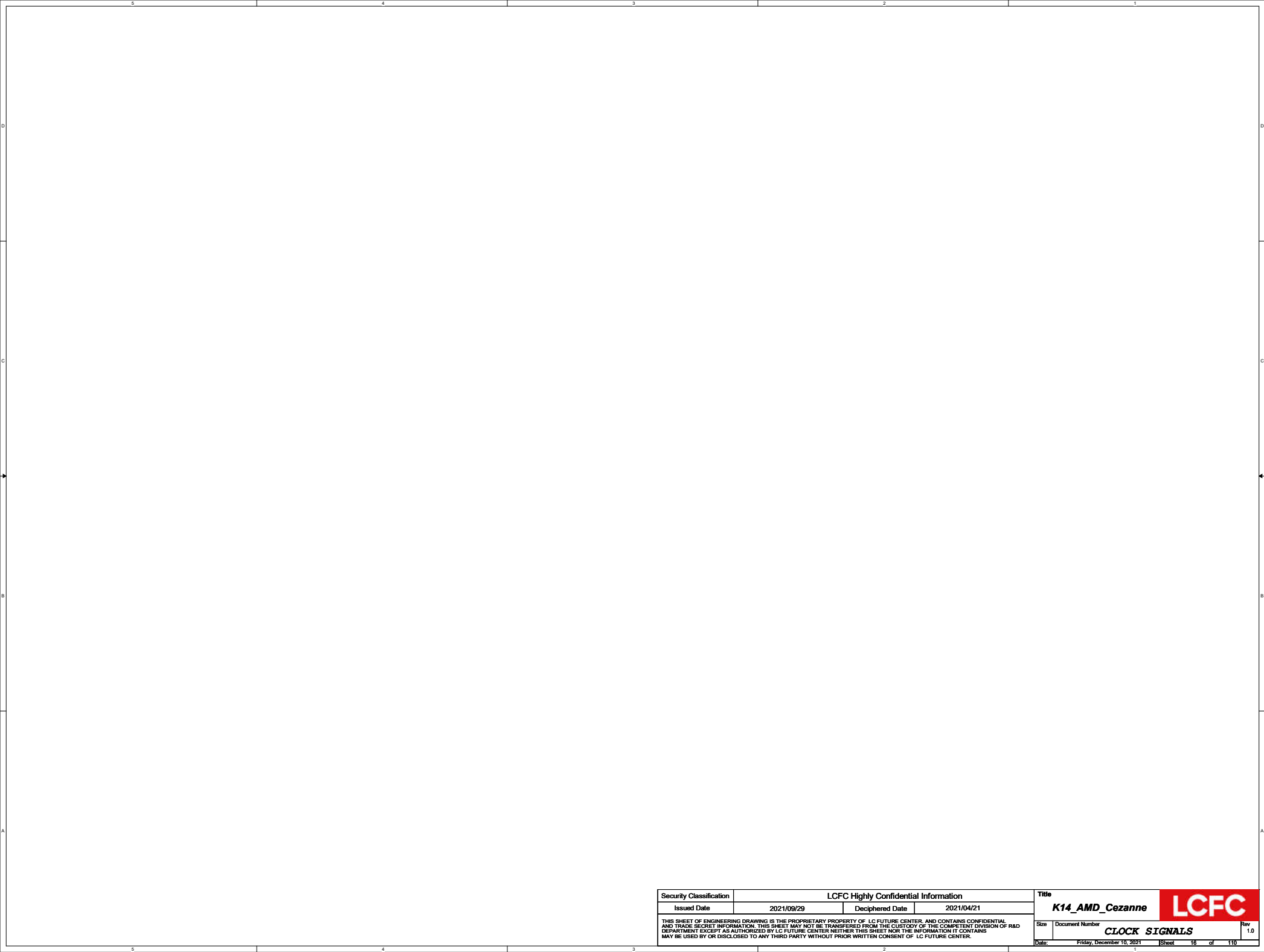


Security Classification				Title	
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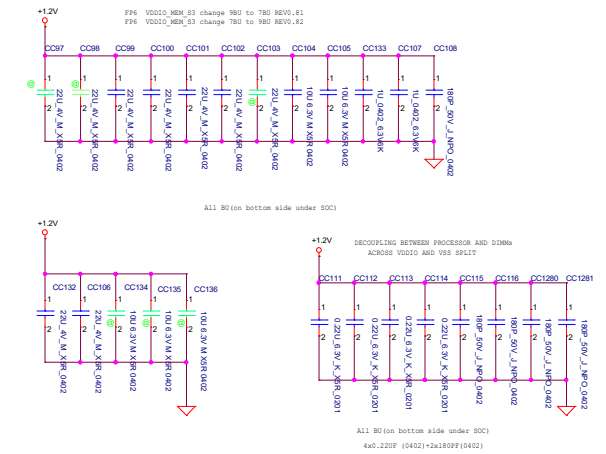
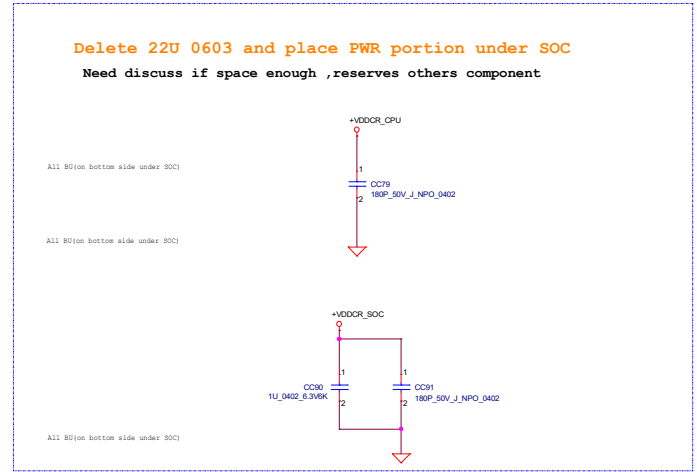
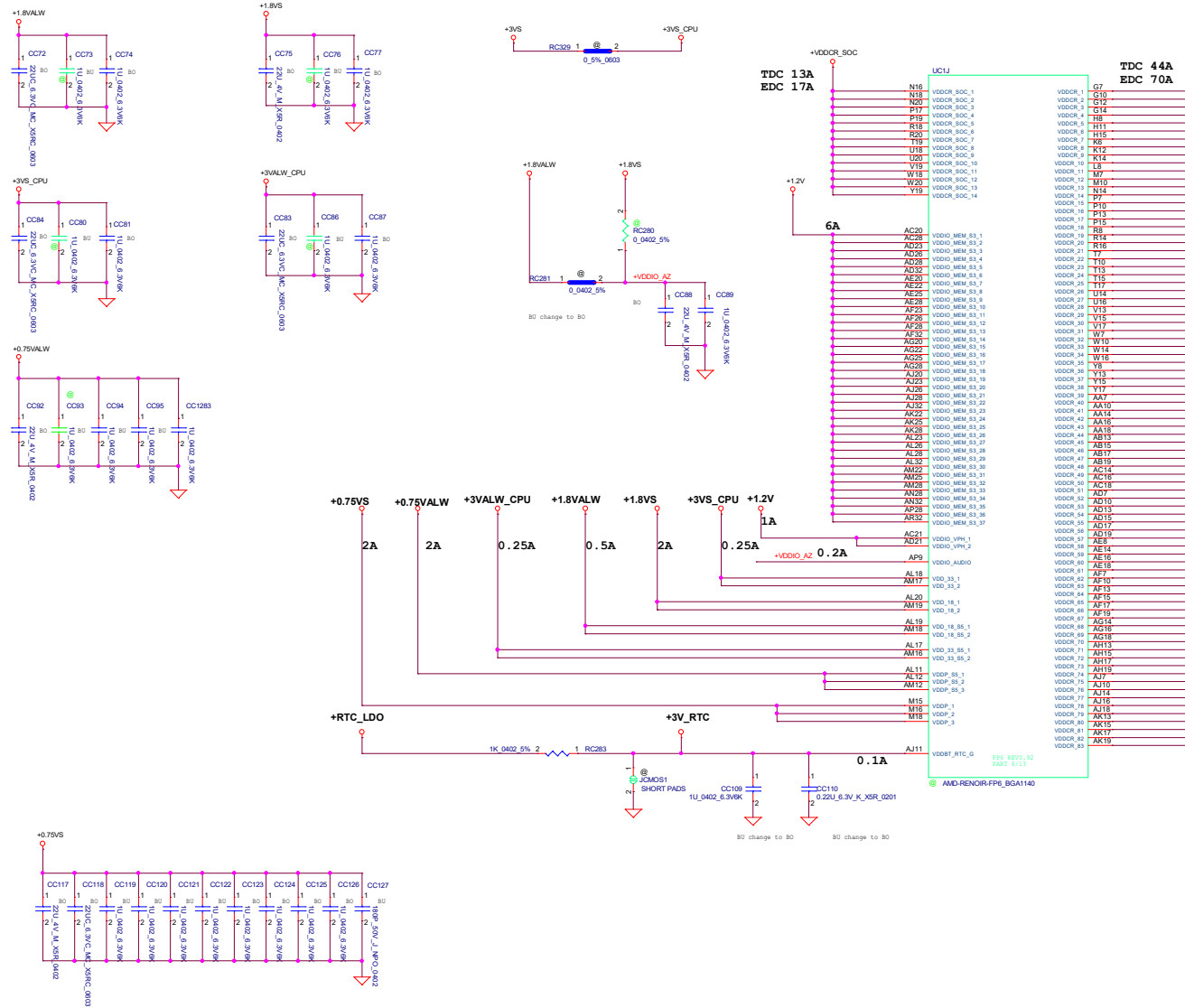


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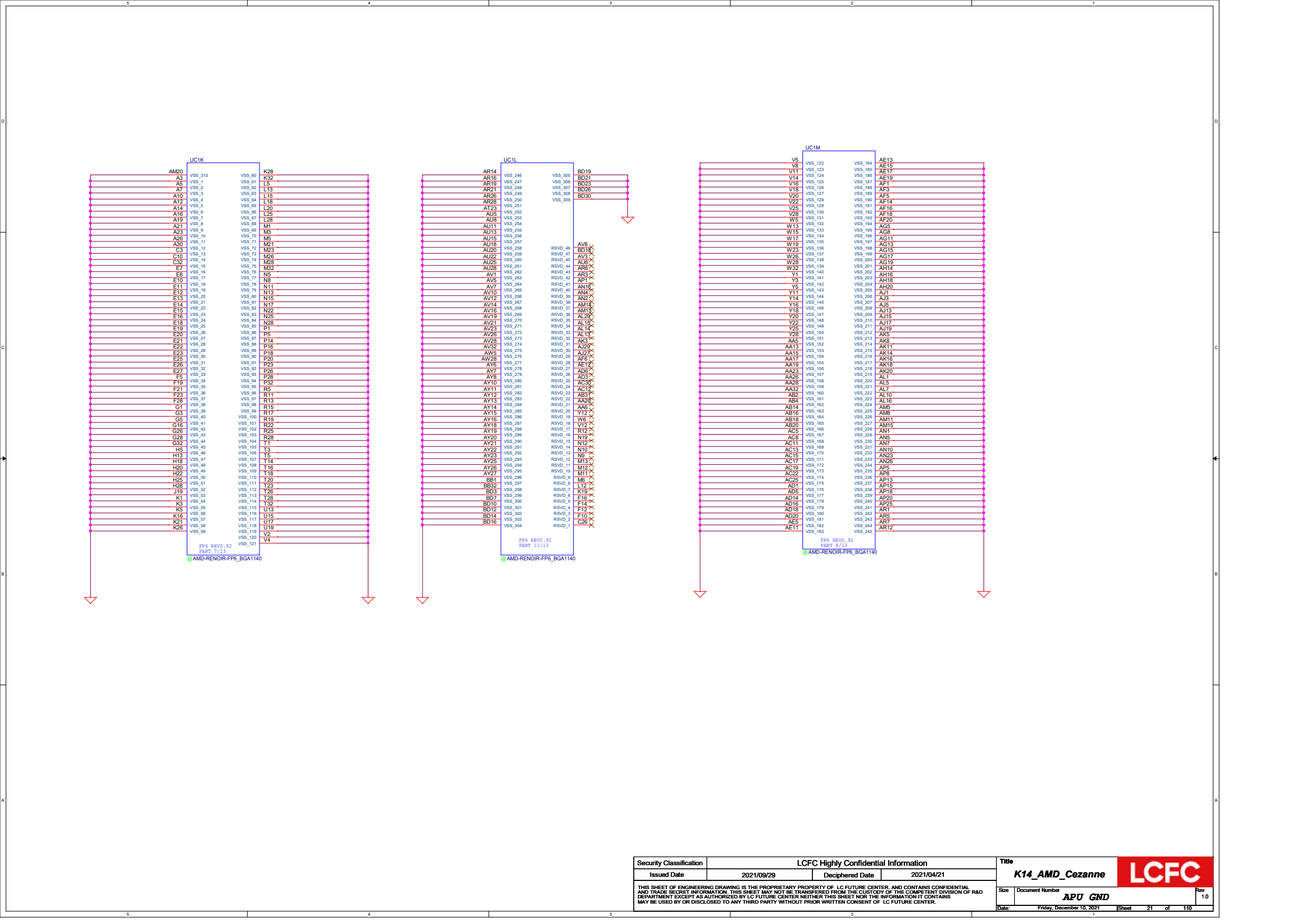
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<div><table><tr><td>Security Classification</td><td colspan="3">LCFC Highly Confidential Information</td><td>Title</td></tr><tr><td>Issued Date</td><td>2021/09/29</td><td>Deciphered Date</td><td>2021/04/21</td><td>K14_AMD_Cezanne</td></tr><tr><td colspan="4">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&amp;D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</td><td>Size</td></tr><tr><td colspan="4"></td><td>Document Number</td></tr><tr><td colspan="4"></td><td>CPU Power(2/2)</td></tr><tr><td colspan="4"></td><td>Rev</td></tr><tr><td colspan="4"></td><td>1.0</td></tr><tr><td colspan="4"></td><td>Date: Friday, December 10, 2021</td></tr><tr><td colspan="4"></td><td>Sheet 19 of 110</td></tr></table><div>LCFC</div></div>					Security Classification	LCFC Highly Confidential Information			Title	Issued Date	2021/09/29	Deciphered Date	2021/04/21	K14_AMD_Cezanne	THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.				Size					Document Number					CPU Power(2/2)					Rev					1.0					Date: Friday, December 10, 2021					Sheet 19 of 110
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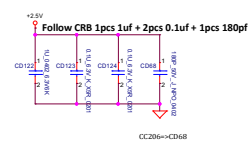
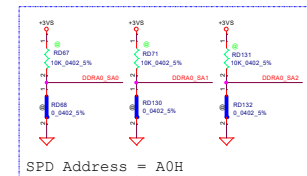
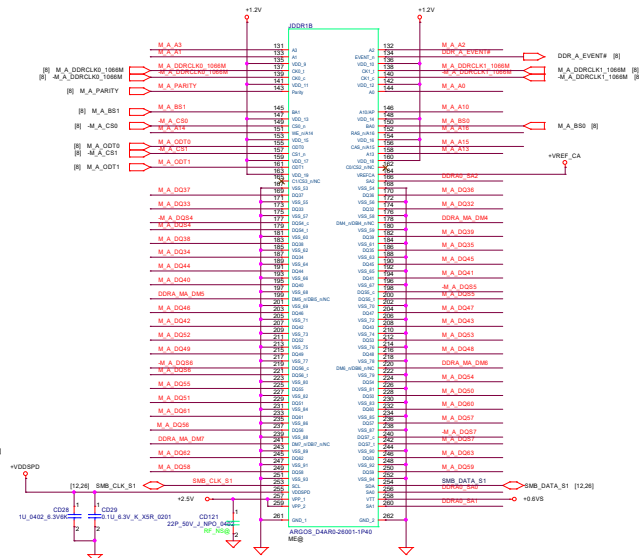




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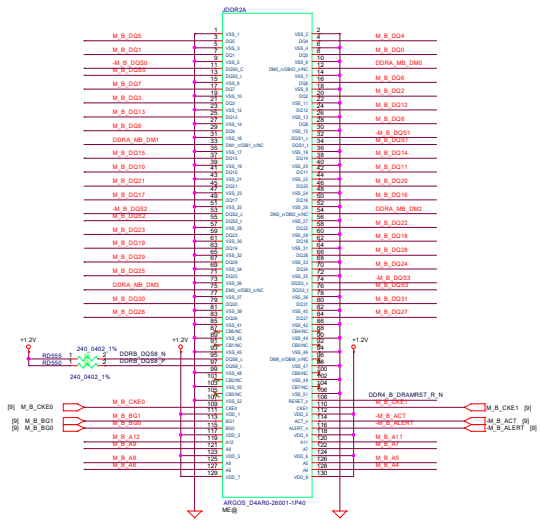
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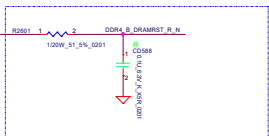




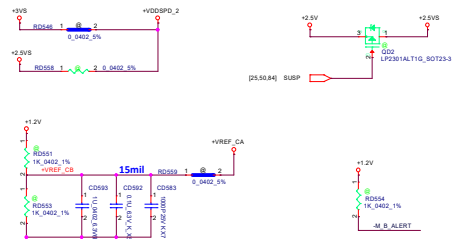
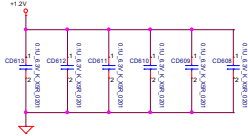
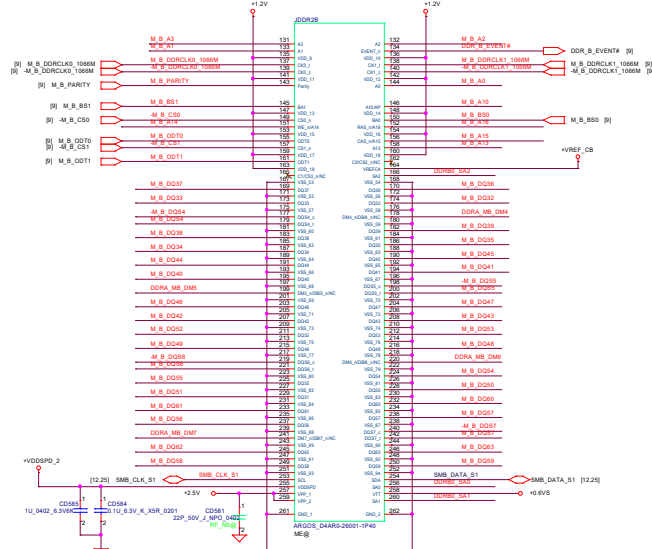
Chage JDDR2 Symbol DC011412251 to SP011508260\_Follow L340 API\_0628



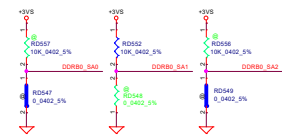
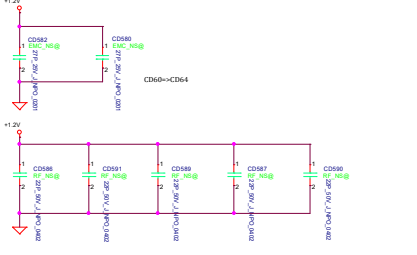
[P] DORA\_R\_DRAMST#  
For MEM\_MB\_RST# overshoot issue



11/11  
Resistor PN from SD000012080 to SD000012087

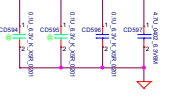


Layout Note: Place near JDDR2

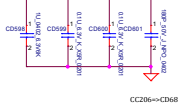


SPD Address = A2H

Follow CRB 1pcs 4.7uf + 1pcs 0.1uf



Follow CRB 1pcs 1uf + 2pcs 0.1uf + 1pcs 180pf



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Rev	D	Document Number	Memory Channel B
Date	20210929	Rev	1

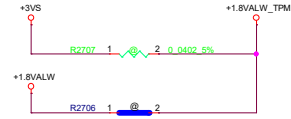
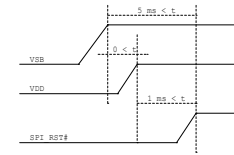


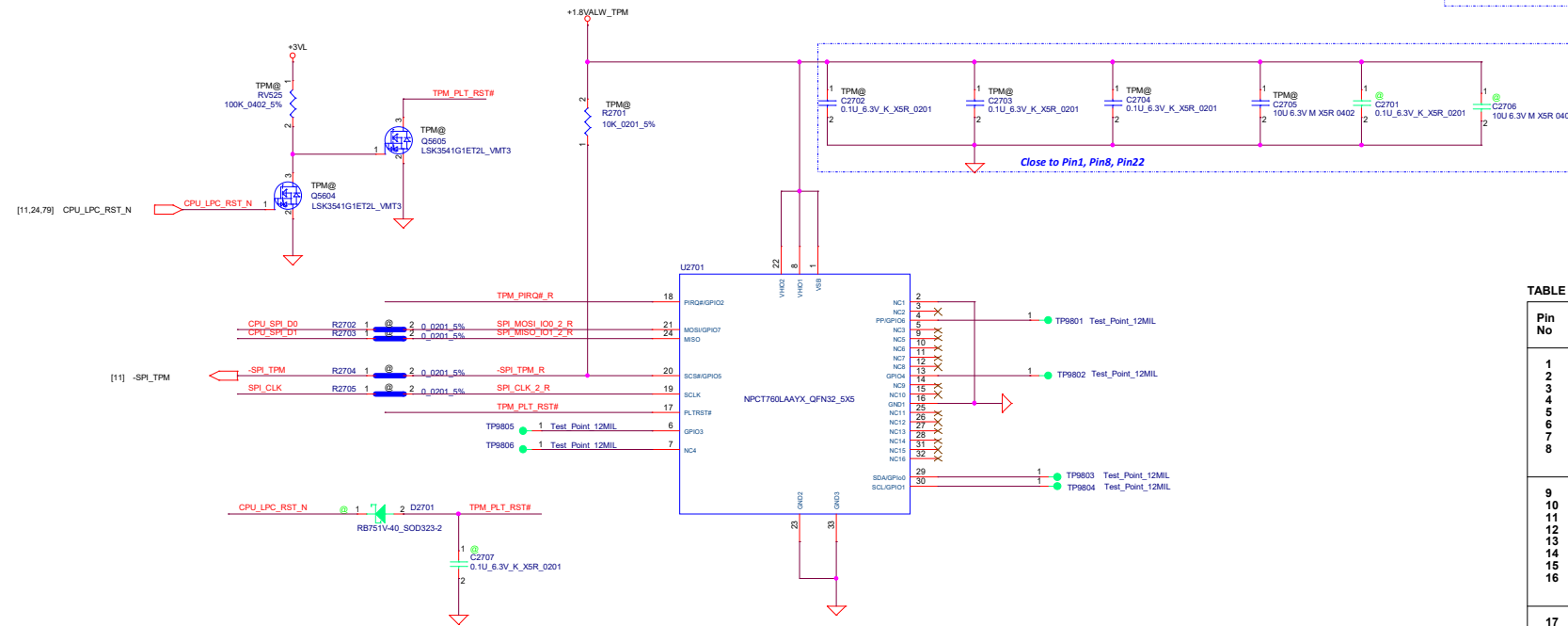
TABLE of TPM (U9801)		
Vendor	P/N	LCFC P/N
Nuvoton	NPCT750LABYX	SA00008KS30
ST Micro	ST33HTPH2X32AHD8	SA00000AB720

NOTE:  
Check timing sequence in SDV phase.



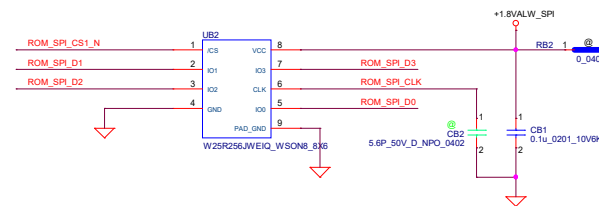
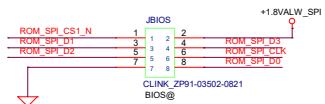
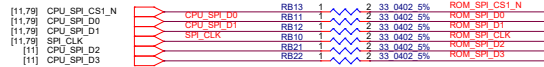
NOTE:

- 1) It is recommended to connect the TPM to the system's standby voltage to improve performance.
- 2) SPI RST# must be asserted for at least 5 msec after VSS power-up.
- 3) VSS may come up anytime before VDD power-up, but not after VDD power-up.
- 4) SPI RST# may be asserted together with VDD power negation, but should not at any point exceed 0.5V above the VDD power level.



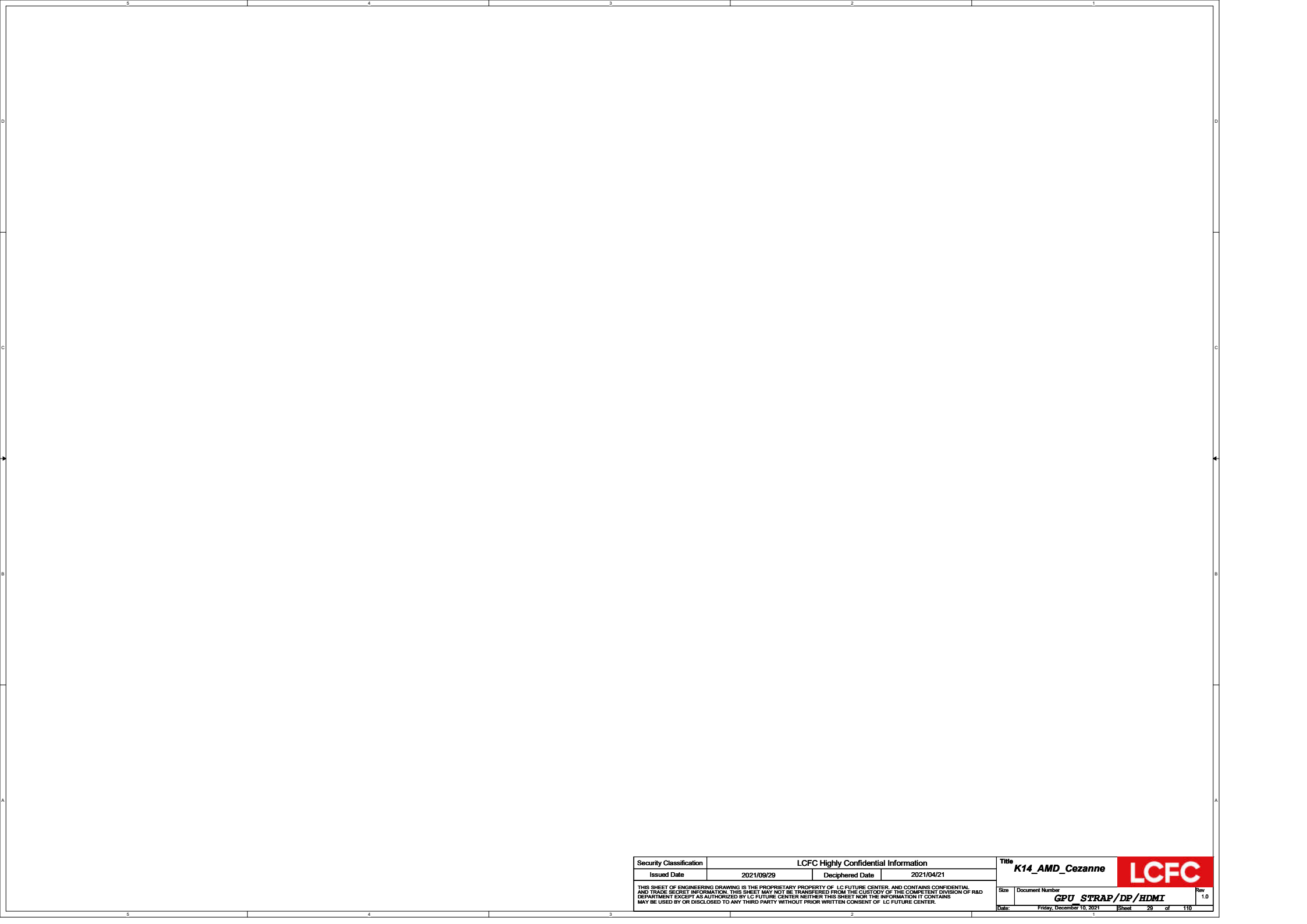
Pin No	TCG PTP Spec (v38)	Nuvoton NPCT750LABYX	ST Micro ST33HPTH2E32AHCO
1	VDD	VSB	NC
2	GND	NC	GND
3	NC	NC	NC
4	GPIO	GPIO/PP	NC
5	NC	NC	NC
6	GPIO	GPIO3	NC
7	GPIO	NC	GPIO
8	VDD	VHIO	NC
9	NC	NC	NC
10	NC	NC	NC
11	NC	NC	NC
12	NC	NC	NC
13	GPIO	GPIO4	NC
14	NC	NC	NC
15	NC	NC	NC
16	GND	GND	NC
17	SPI_RST#	RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#/GPIO2	SPI_PIRQ#
19	SPI_CLK	SCLK	SPI_CLK
20	SPI_CS#	SCS#/GPIO5	SPI_CS#
21	MOSI	MOSI/GPIO7	MOSI
22	VDD	VHIO	VPS
23	GND	GND	NC
24	MISO	MISO	MISO
25	NC	NC	NC
26	NC	NC	NC
27	NC	NC	NC
28	NC	NC	NC
29	SDA/GPIO1	SDA/GPIO1	NC
30	SDA/GPIO0	SDA/GPIO0	NC
31	NC	NC	NC
32	NC	NC	NC


## SPI ROM



5	4	3	2	1																																													
D				D																																													
C				C																																													
B				B																																													
A				A																																													
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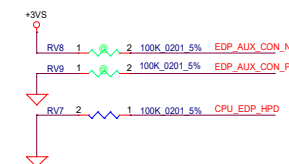
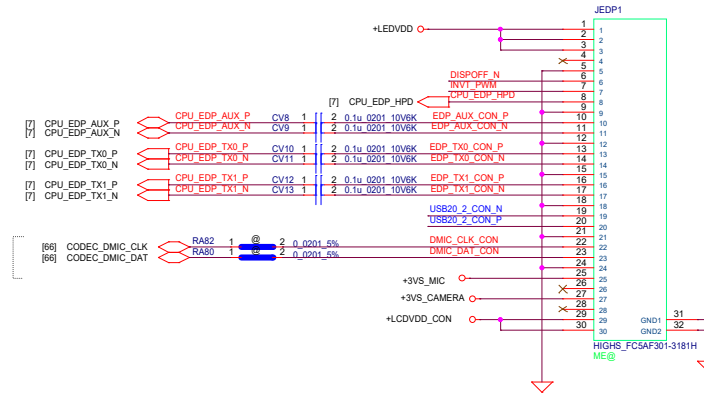
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Diagram illustrating the input stage of the CA96 op-amp. The non-inverting input (+) is connected to a voltage divider consisting of a 10k resistor (R1) and a 100k resistor (R2) connected to +3V5\_MIC. The inverting input (-) is connected to a voltage divider consisting of a 10k resistor (R3) and a 100k resistor (R4) connected to +3V5\_MIC. The output of the op-amp is connected to a 10k resistor (R5) and a 100k resistor (R6) connected to +3V5\_MIC. The op-amp is labeled CA96 and has a gain of 10. The input signal is labeled W=40mils.



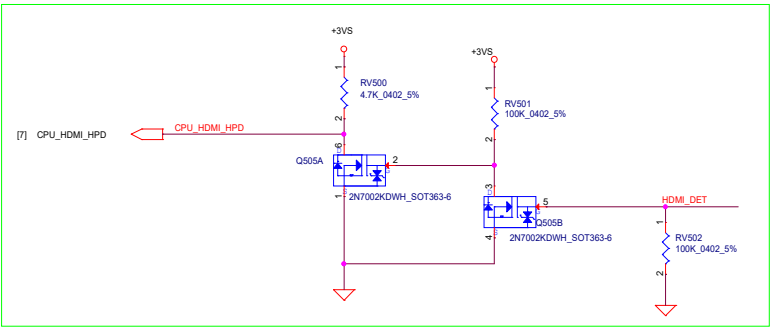
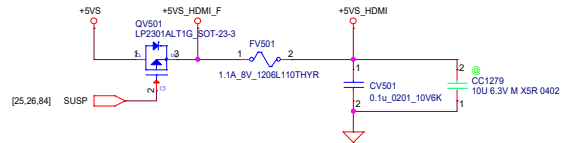
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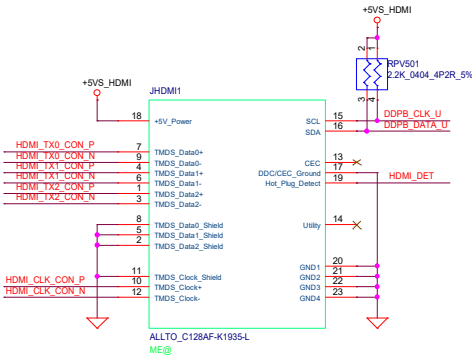
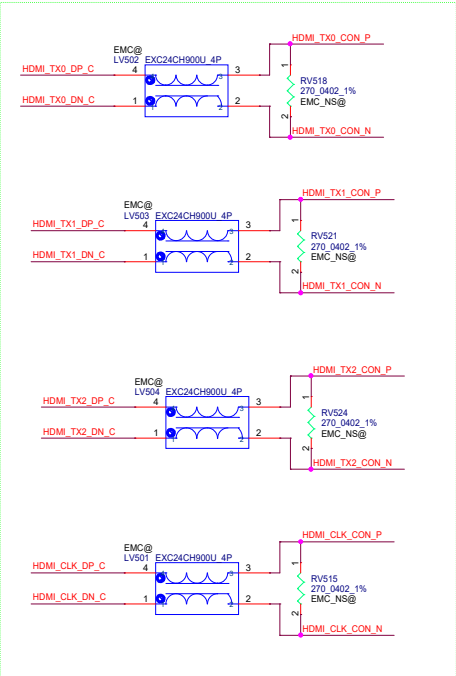




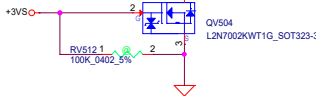
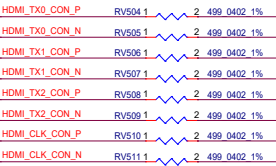
HDMI Power



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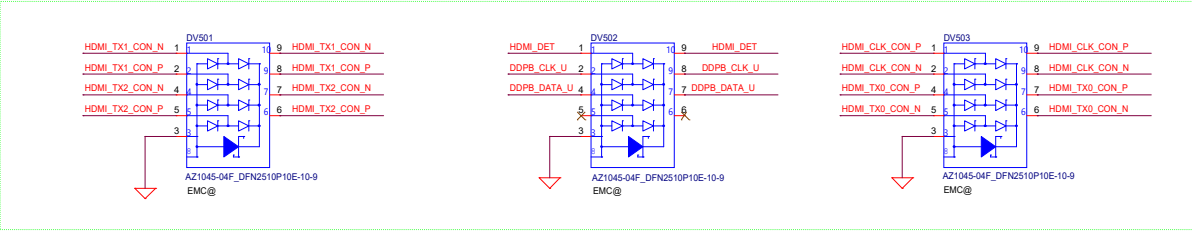


common desing: Rtrnds 470R, On CAP with Common choke \_0630



Need to APU Pull highg R

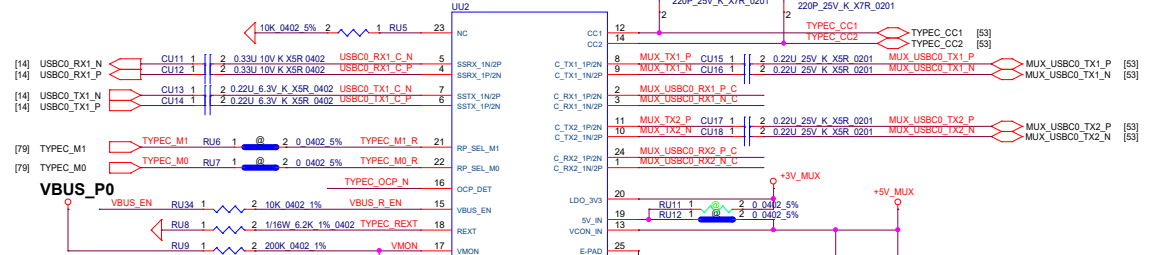
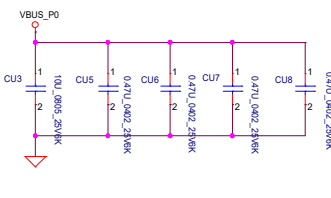
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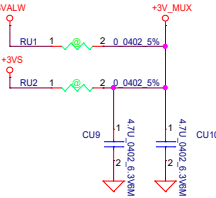


+5VALW



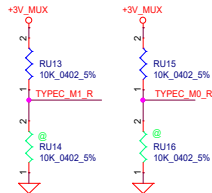
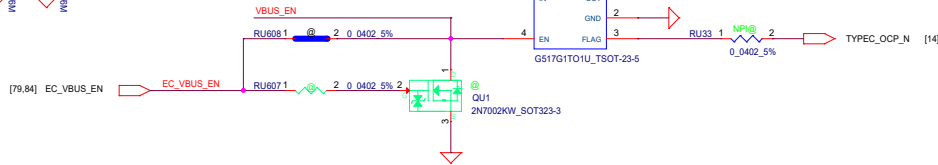
Change RU34 0R to 10K,  
ADD Ec control Power output\_SIT 0921

3. 4A



+5VALW

VBUS\_P0



Rp Configuration  
Rp:3A (NOW)

	M1	M0	Note
Rp:900mA	0	1	RU14/RU15 mount
Rp:1.5A	1	0	RU13/RU16 mount
Rp:3.0A	1	1	RU13/RU15 mount

For C\_VBUS  
Power Switch Enable Pin

Power Switch Enable PIN	Note
Low Active	RU17 mount
High Active	RU18 mount

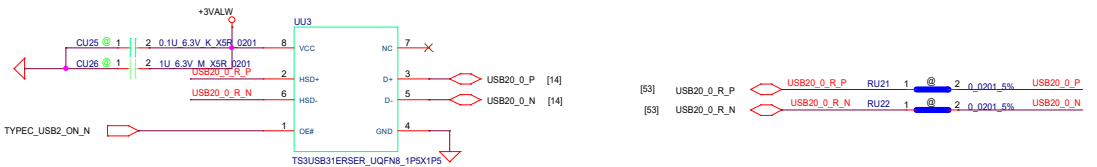
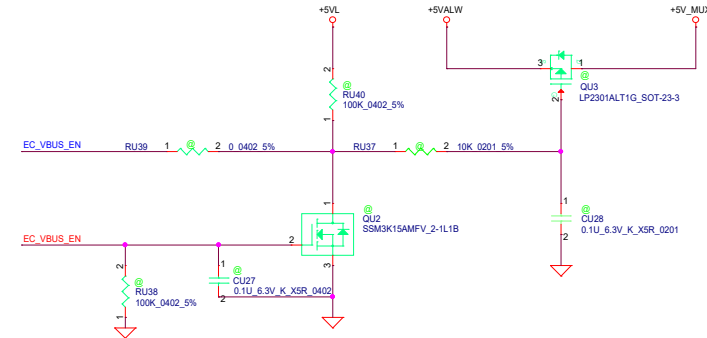
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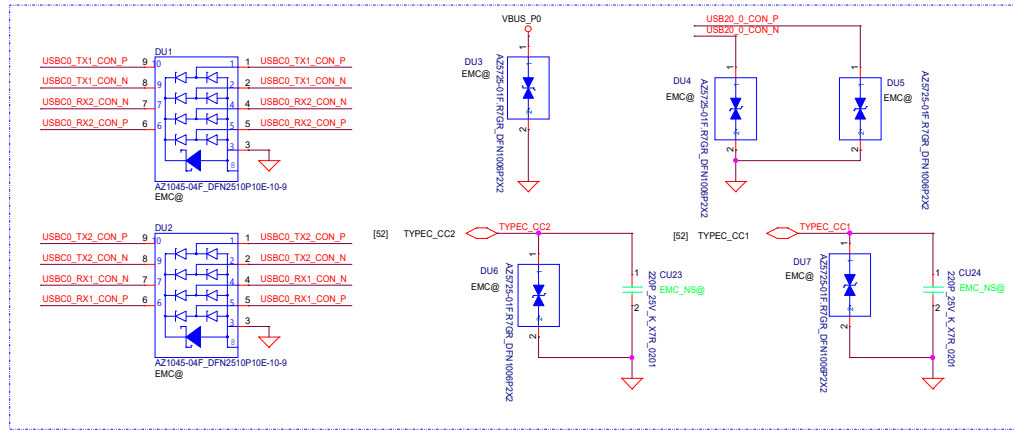
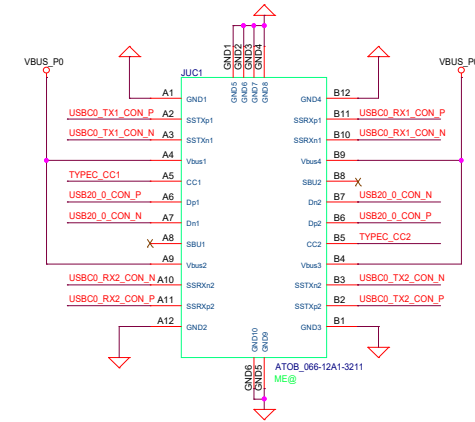
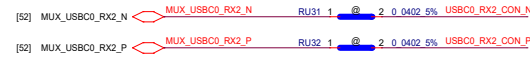
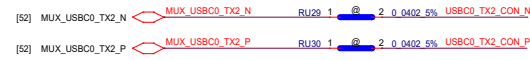
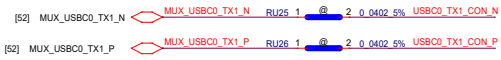
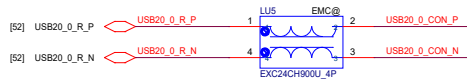
For C\_VBUS  
Power Switch OCP Pin

Power Switch OCP PIN	Note
Low Active	RU19 mount
High Active	RU20 mount

SVT change RU19 unstuff to stuff for solve DC S5 to S0 U DISK LOSS\_1204

Add reserved MUX power control\_0926







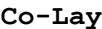
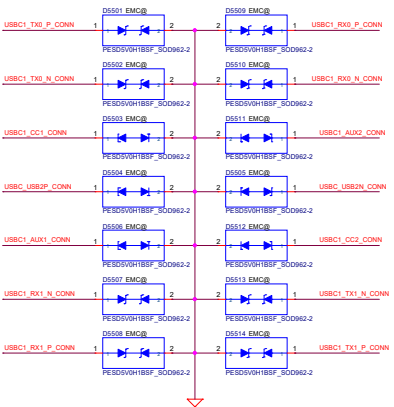


TABLE of EMC TVS (D6301~D6314)		
Vendor	LCFC P/N	Description
NXP	SC400008300	S DIO_ESD PESD5V0H1BSF SOD962
AMAZING	SC400009F00	S DIO_ESD AZ5B6S-01B.R7G CSP0603P2Y



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Size	Document Number				Rev 1.0
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Date	Friday, December 16, 2021		15:46	65	of 116

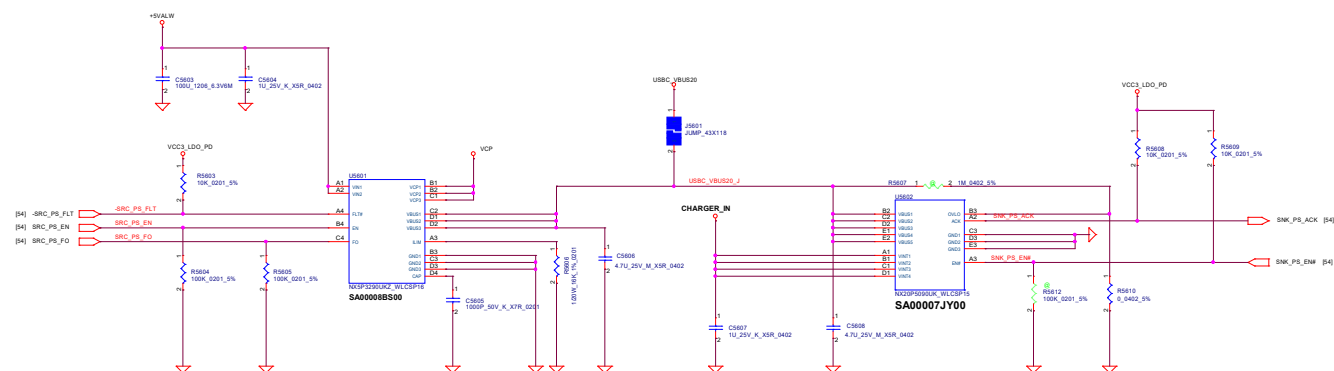


TABLE of TypeC Load Switch (U5602)		
Vendor	LCFC P/N	P/N
NXP	SA00007JY00	NX20P5090UKAZ
KINETIC	SA00009G700	KTS1677EVH-TR



## USB3.0 PORT Close to USB Conn

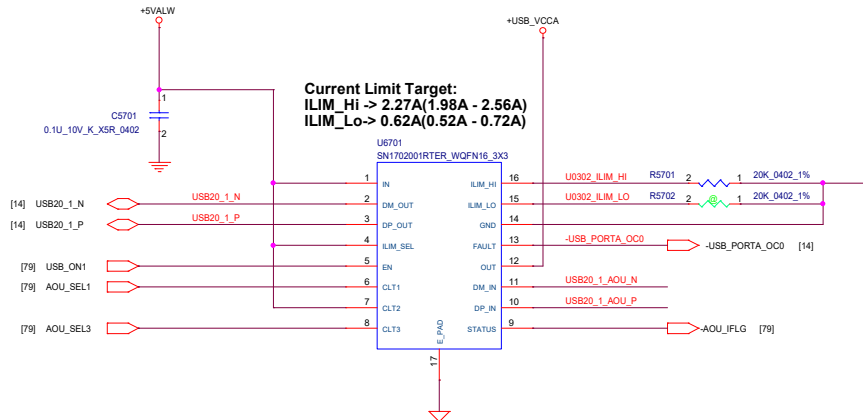
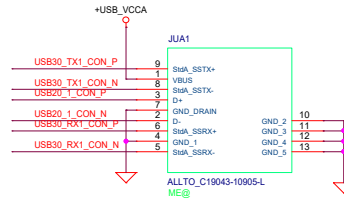
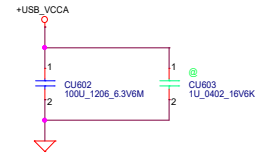
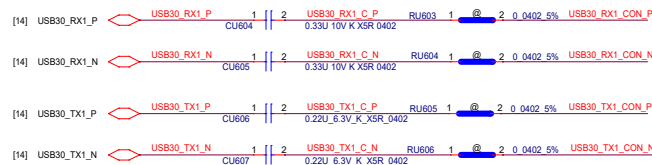
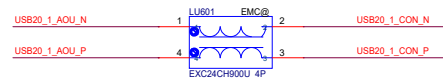
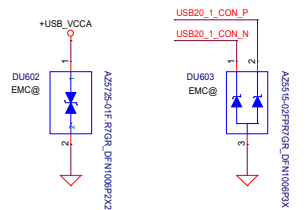
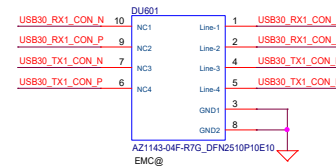


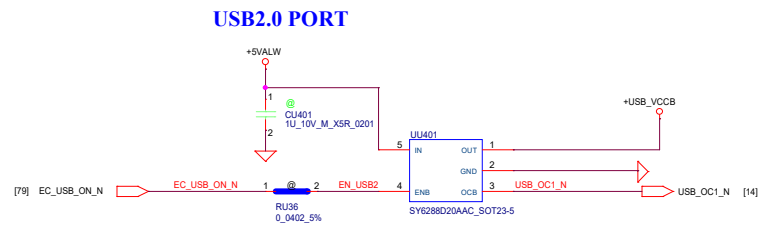
TABLE of POWER SWITCH (U6401)		
Vendor	LCFC P/N	Description
TI	SA00008HF00	S IC SN1702001RTER WQFN 16P USB CHARGING
DIODES	SA00009D800	S IC PI5USB2546HZHEX TQFN 16P CONTROLLER



## EMC Close to USB Conn

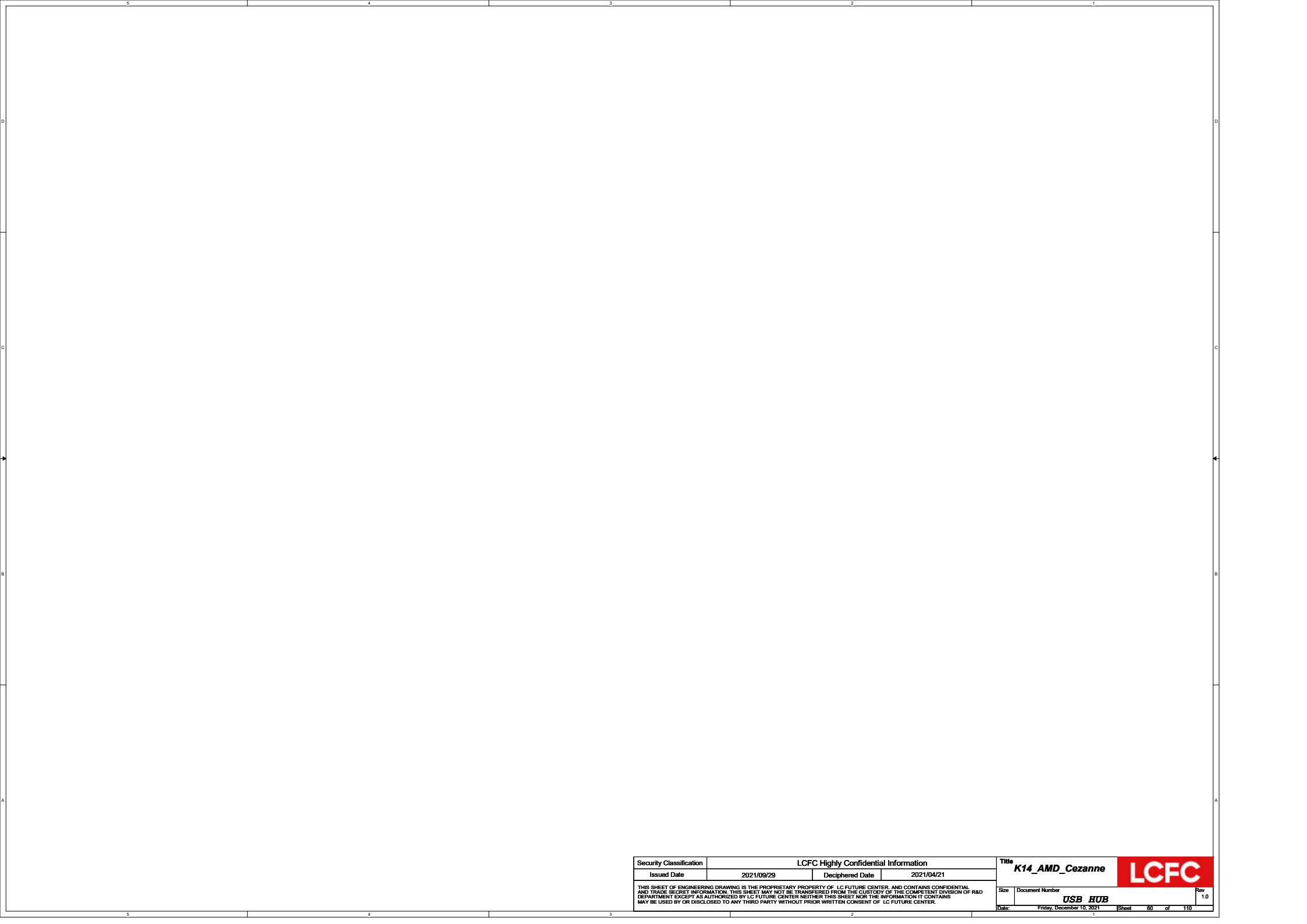



USB2.0 Port and CMC&TVS&CAP MOVE to SUB Board



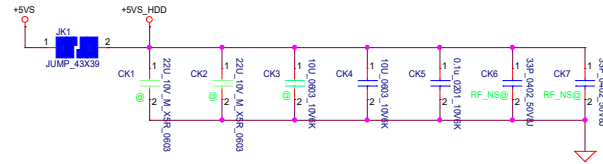
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Issued Date		2021/09/29		Deciphered Date		2021/04/21					
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Size		Document Number								Rev	
Date		Friday, December 10, 2021								Sheet 58 of 110	
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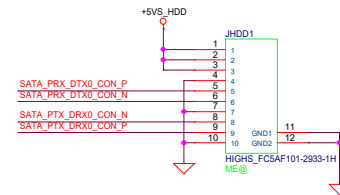
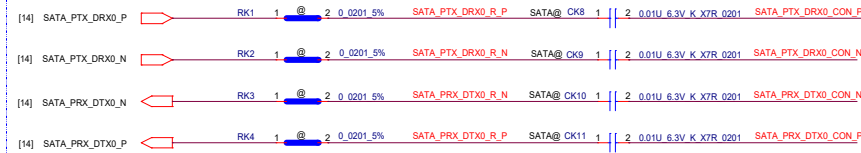


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					USB_HUB	Rev 1.0
				Date:	Friday, December 10, 2021	Sheet 60 of 110

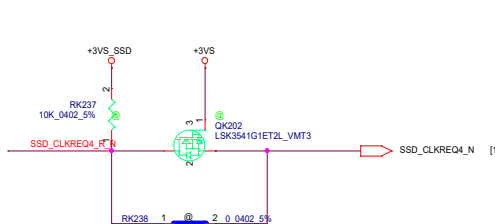
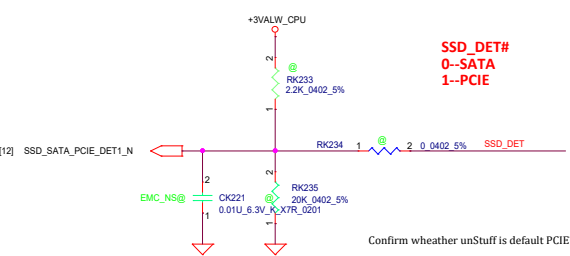
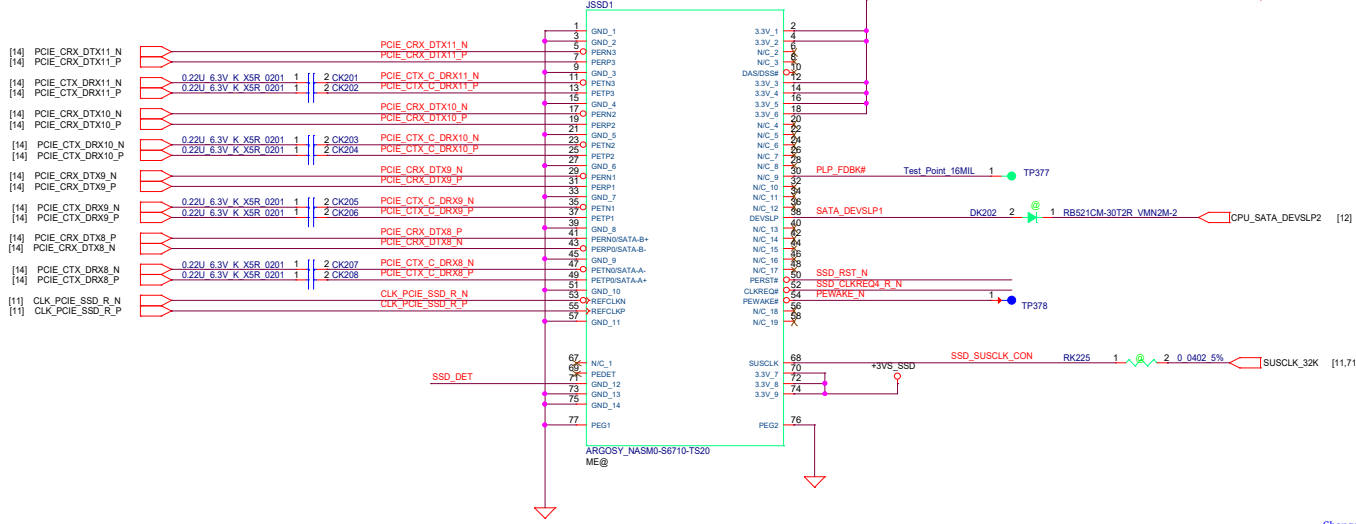
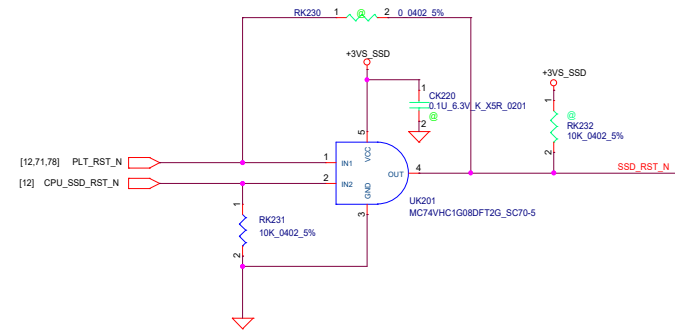
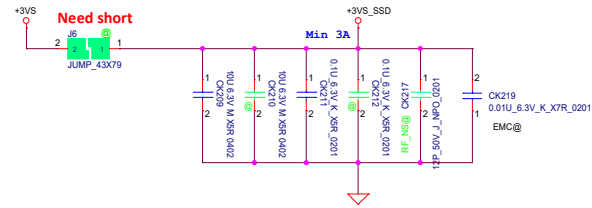
# HDD Power



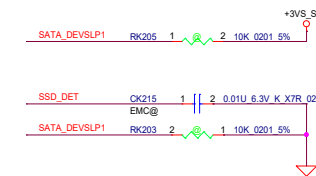
## HDD Without Redriver







Change CK215 0.01U unstuff to 0.01F stuff EMC Require\_20201203

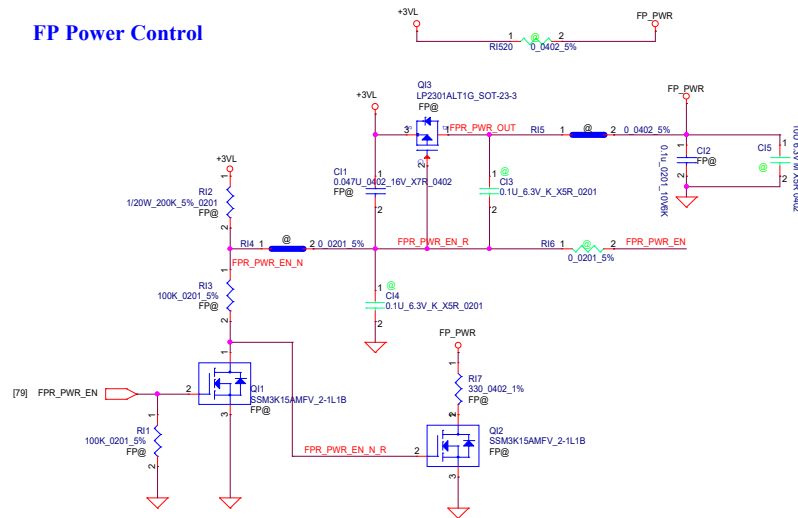


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Date: Friday, December 10, 2021 Sheet 64 of 110																																												





## FP Power Control



FingerPrint USB2.0==>APU USB2.0\_6

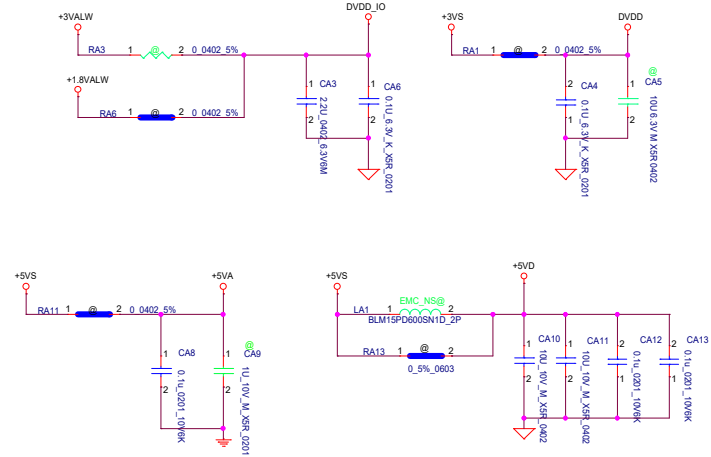
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[14] USB20\_6\_P USB20\_6\_P R19 1 @ 2 0 0402 5% USB20\_6\_CON\_P USB20\_6\_CON\_P [78]

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		C		FP_PWR	1.0
Date:		Friday, December 10, 2021	Sheet	65	of 110

**LCFC**

Note: DVDD-IO must be equal to or smaller than DVDD



[69] HPOUT\_L  
[69] HPOUT\_R

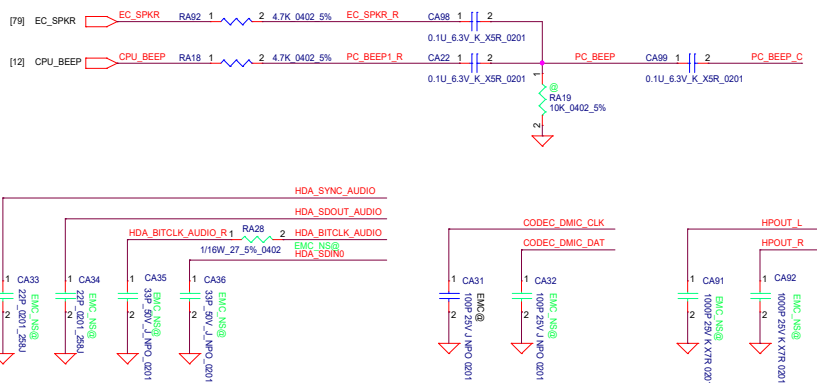
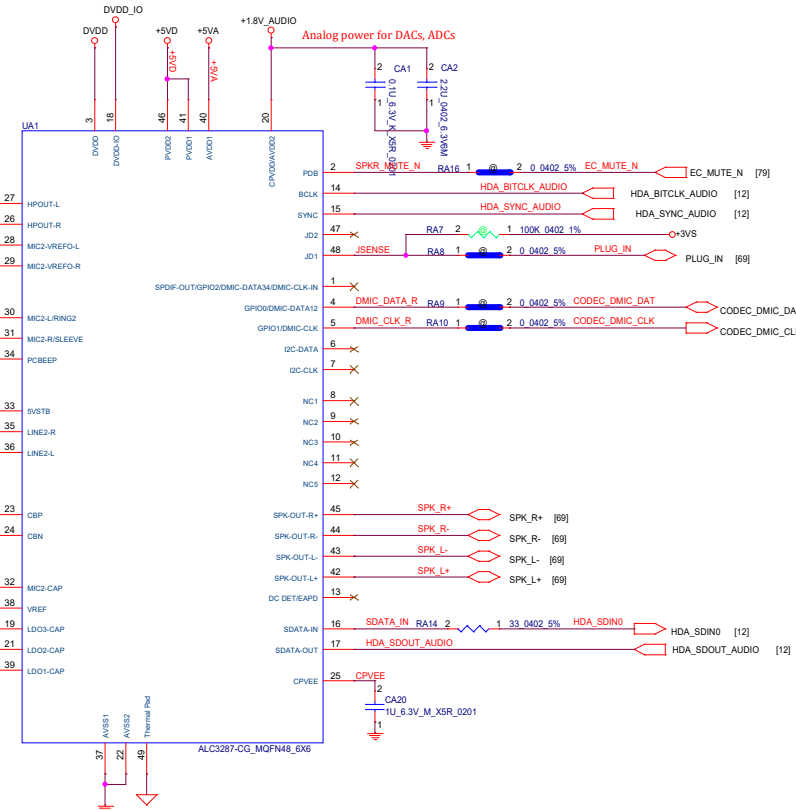
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[69] HPOUT\_R  
[69] MIC2\_VREFOL  
[69] MIC2\_VREFOR  
[69] RING2\_CONN  
[69] RING3\_CONN  
[69] PC\_BEEP\_C  
[69] LINE2-R  
[69] LINE2-L

CA14

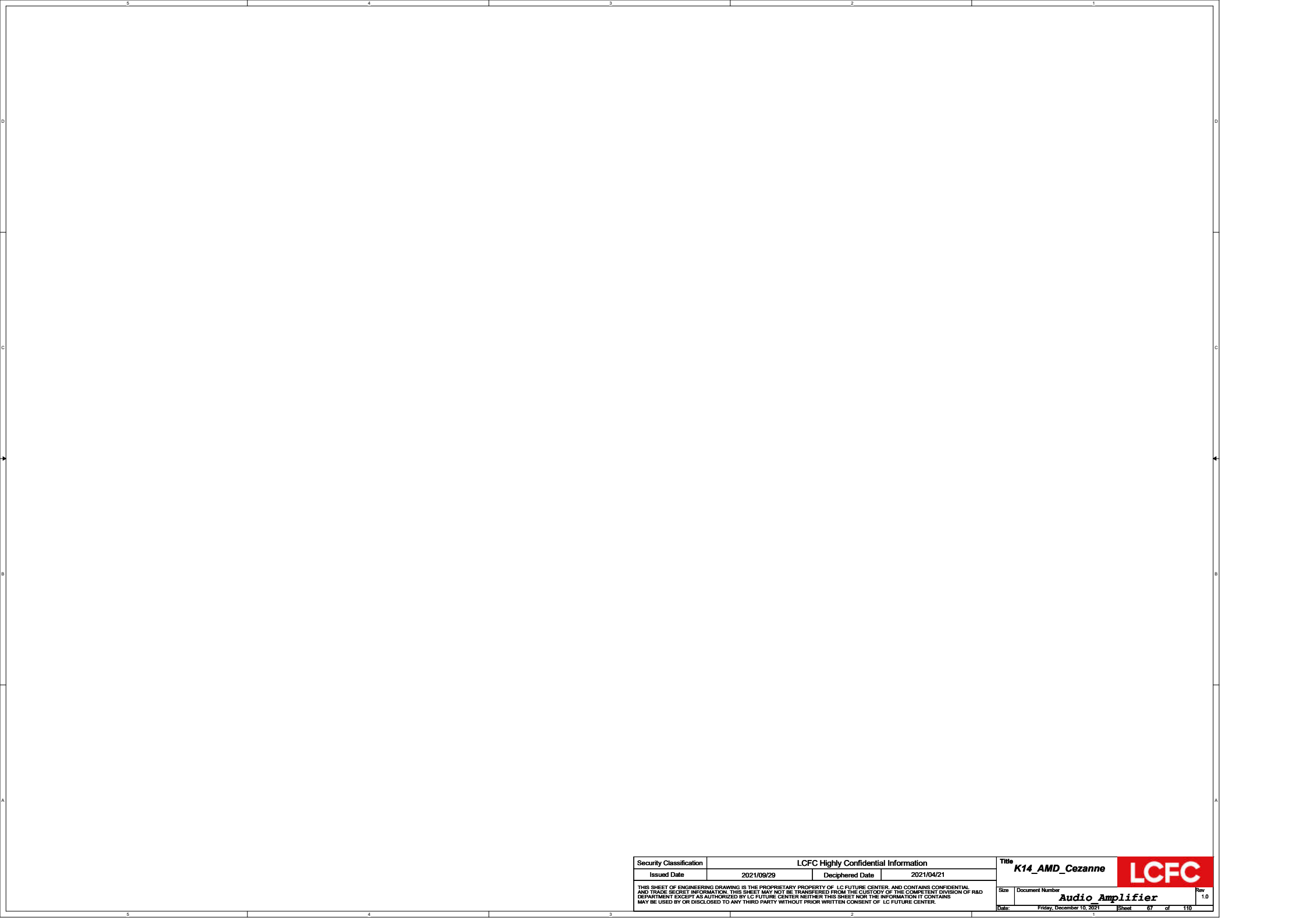
CA15  
CA16  
CA17  
CA18  
CA19


MIC2-CAP  
VREF  
LD03-CAP  
LD02-CAP  
LD01-CAP

CA91, CA92 Is it necessary to reserve



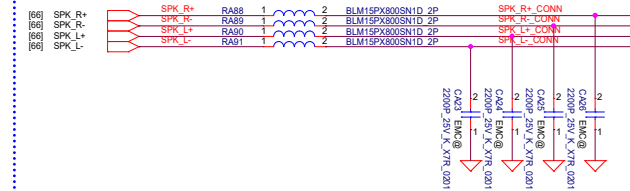
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Audio Codec					1.0
Date:	Friday	August 0, 2021	Sheet	65	of 110



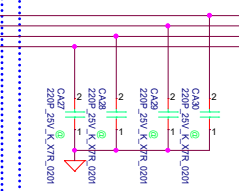
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				Date:	Friday, December 10, 2021	Sheet	67	of	110



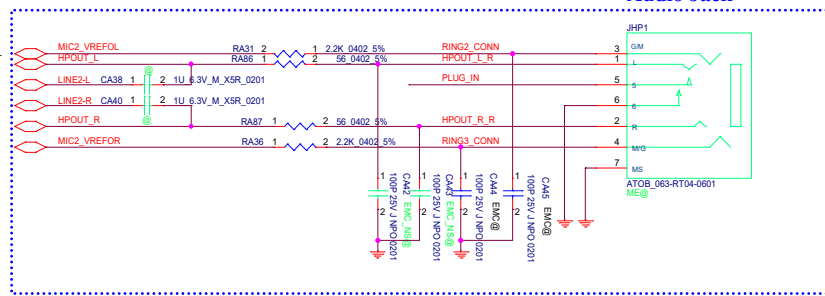
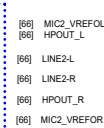
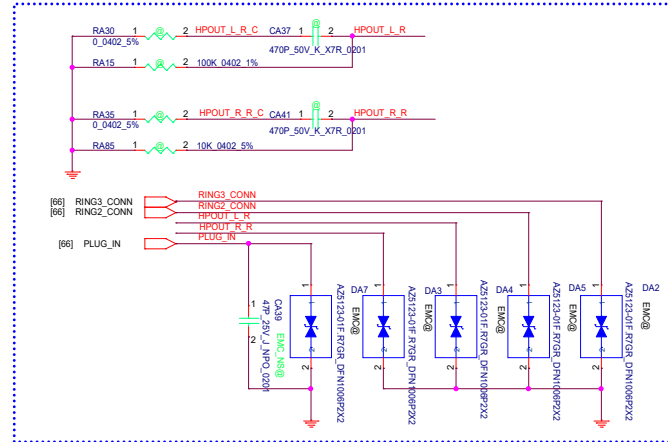
# For EMC Near CODEC



# For EMC Near Conn.

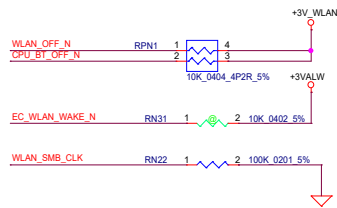



# For EMI



2021/11/11  
Fix Audio test issue

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2									
3									
4									




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				Date:	Friday, December 10, 2021	Sheet	71 of 110	





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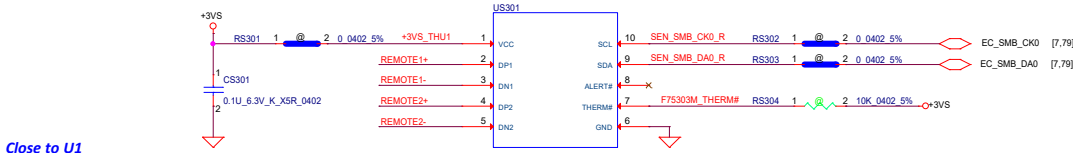


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				Size		Document Number	Rev
						LAN CONN	1.0
				Date:		Friday, December 10, 2021	Sheet 75 of 110



APU Thermal Sensor

Thermal Sensor  
placed nearby SO-DIMM



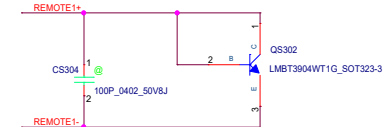
Close to U1



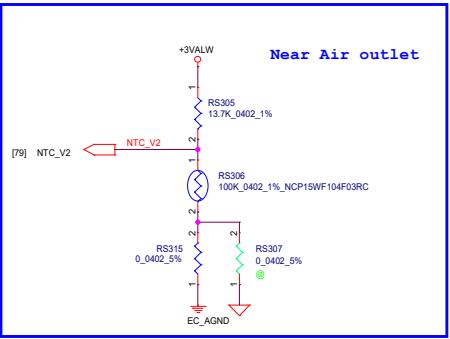
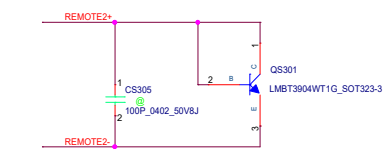
Address 1001\_101xb  
Internal pull up 1.2K to 1.5V  
R for initial thermal shutdown temp

REMOTE2+/-:  
Trace width/space:10/10 mil  
Trace length:<8"

Close to Charger

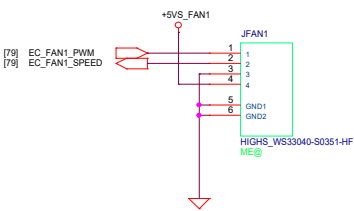
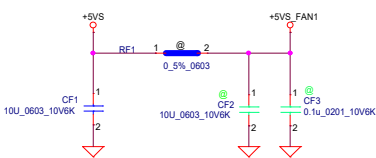


Close APU



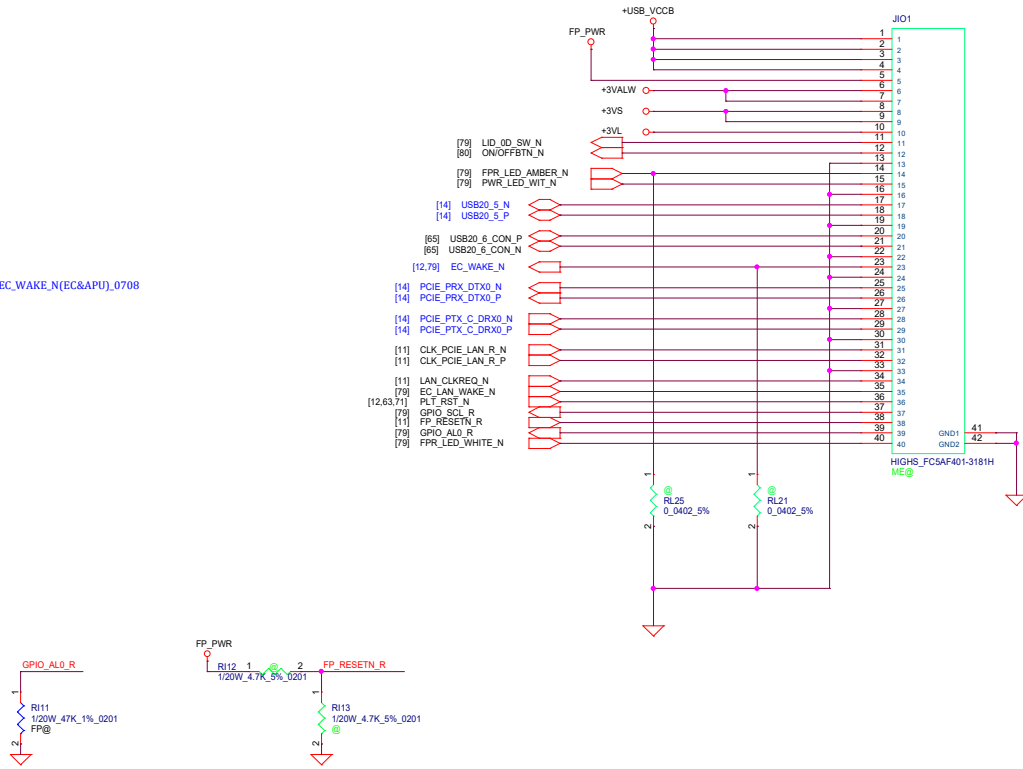
Near Air outlet

FAN

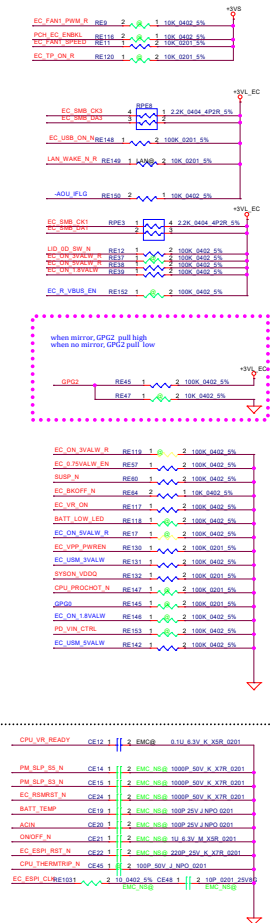
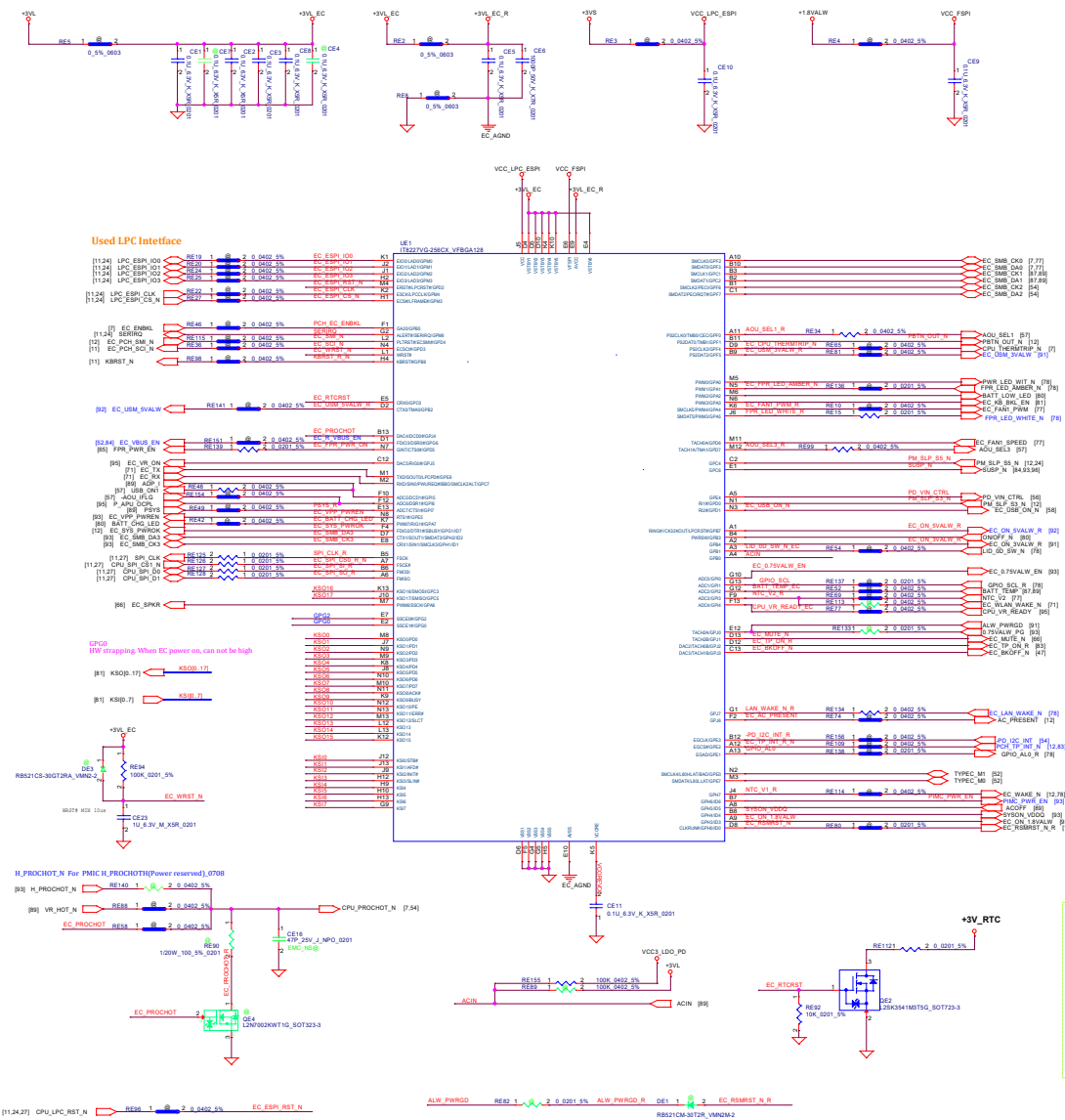


FPC+Cable+Wire

PIN23 Intel is PCH\_LAN\_WAKE\_N  
AMD IO Boad ReserD OR to this PIN:EC\_WAKE\_N(EC&APU).0708



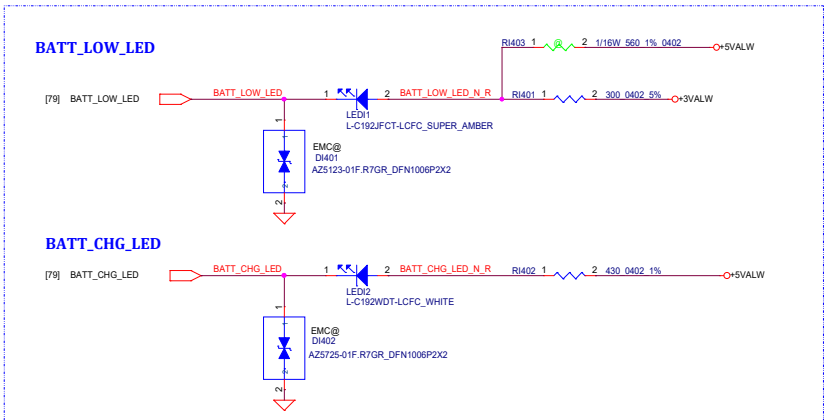
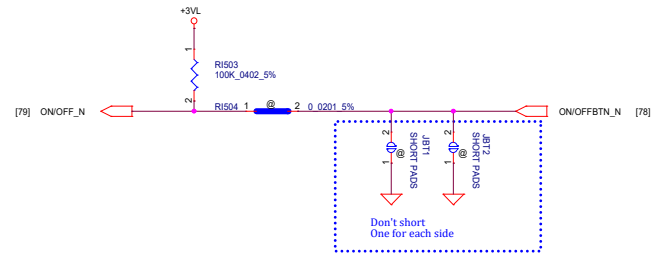
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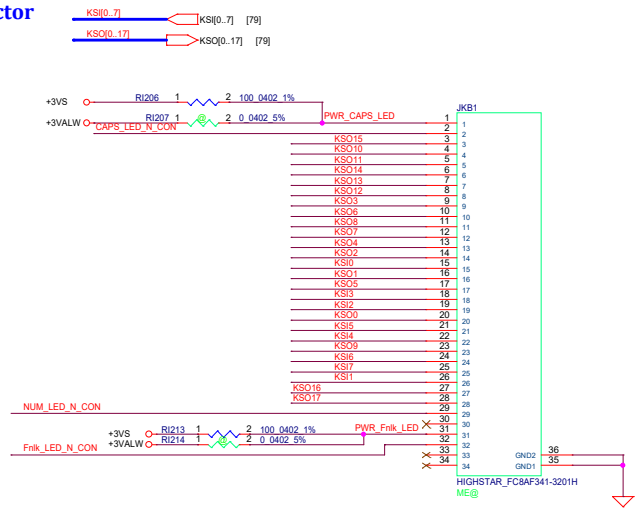
PWR BUTTON

LED	State	LED Behavior
Power Button	System on	White_ON(Battery: 21%~100%)
	Standby LID closed	Amber_ON(Battery: 0%~20%)
	System off	White_ON(Battery: 21%~100%)
	System off	OFF
Charging	Battery only	OFF
	Charging	Amber_ON(Battery: 1%~90%) White_ON(Battery: 91%~100%)

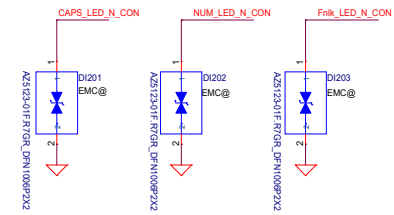
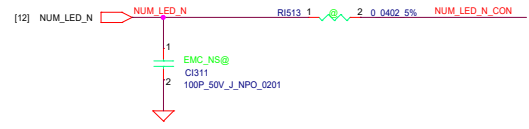
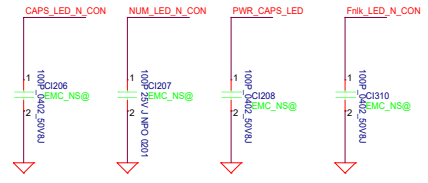
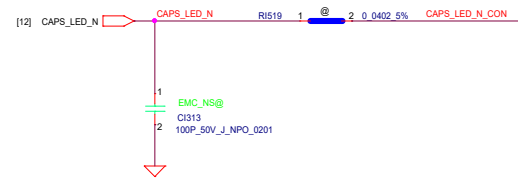
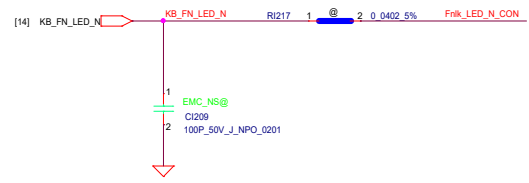
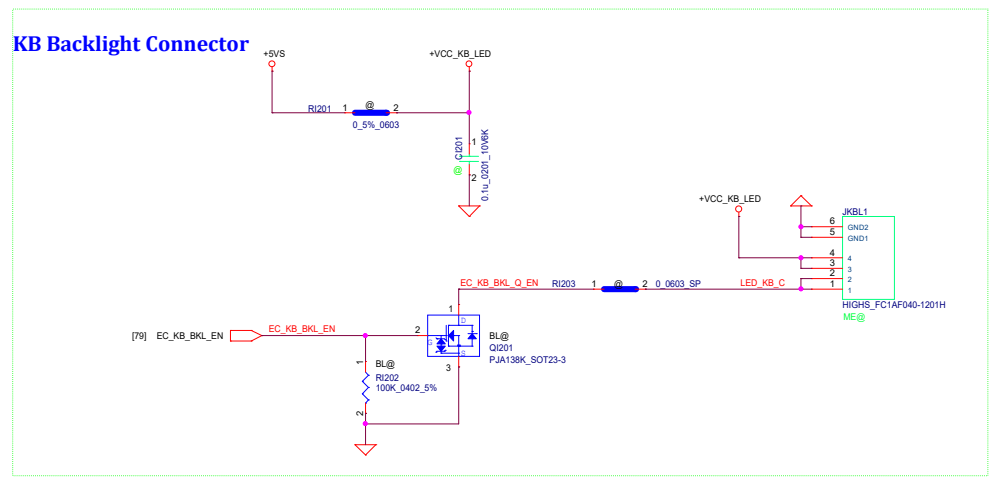




K/B Connector

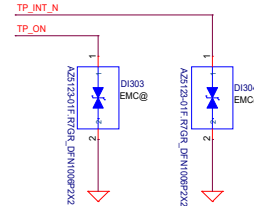
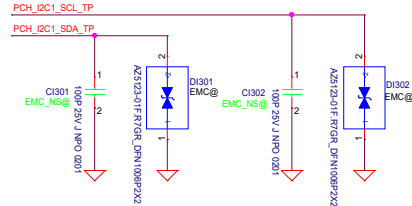
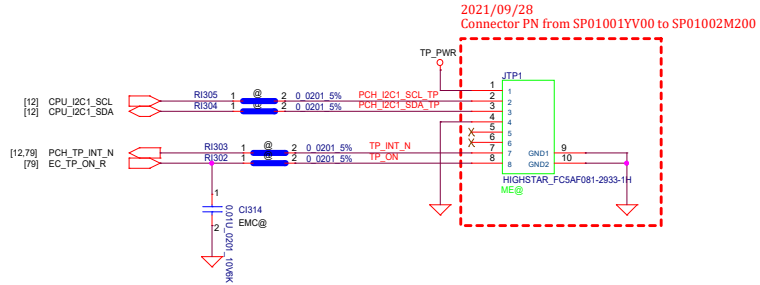
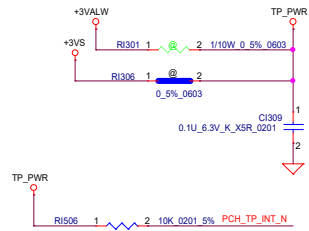


KB Backlight Connector

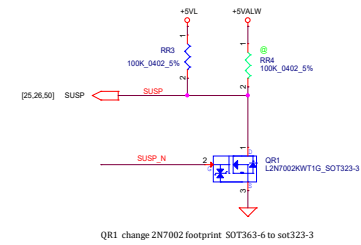
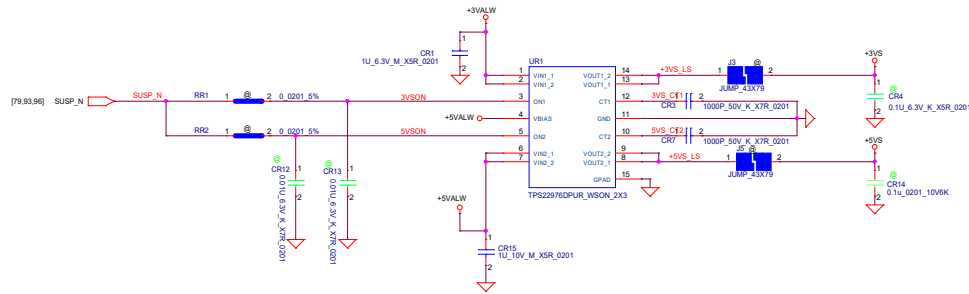




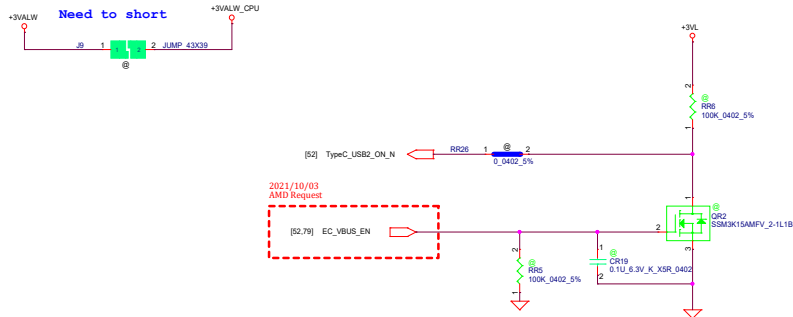
# Touch Pad



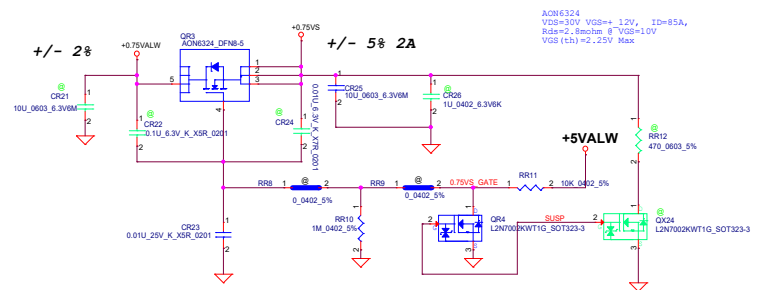
### 3VS/5VS



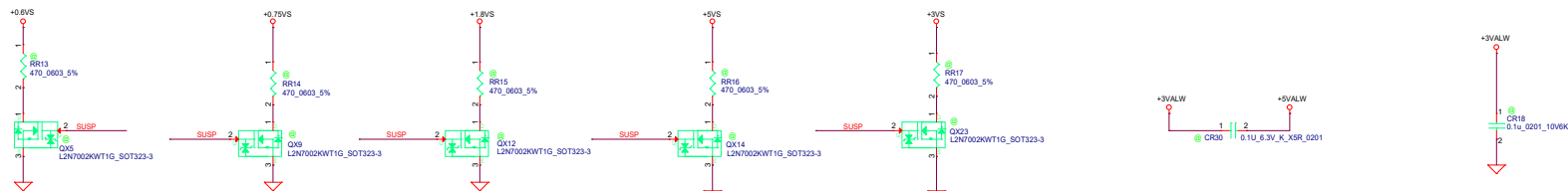
### TO +3VALW\_APU



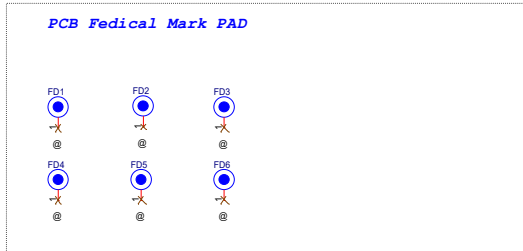
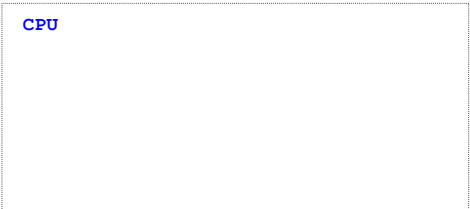
### TO +0.75VS



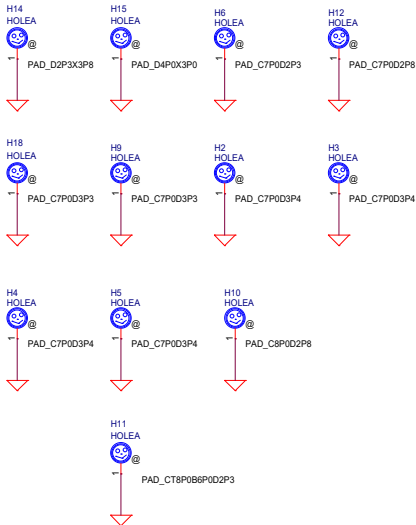
### For DisCharge



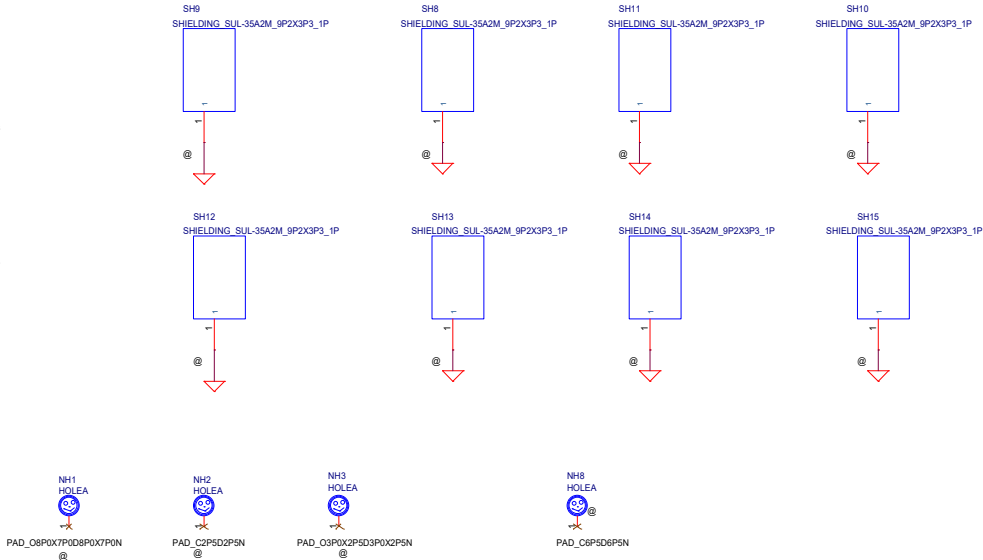
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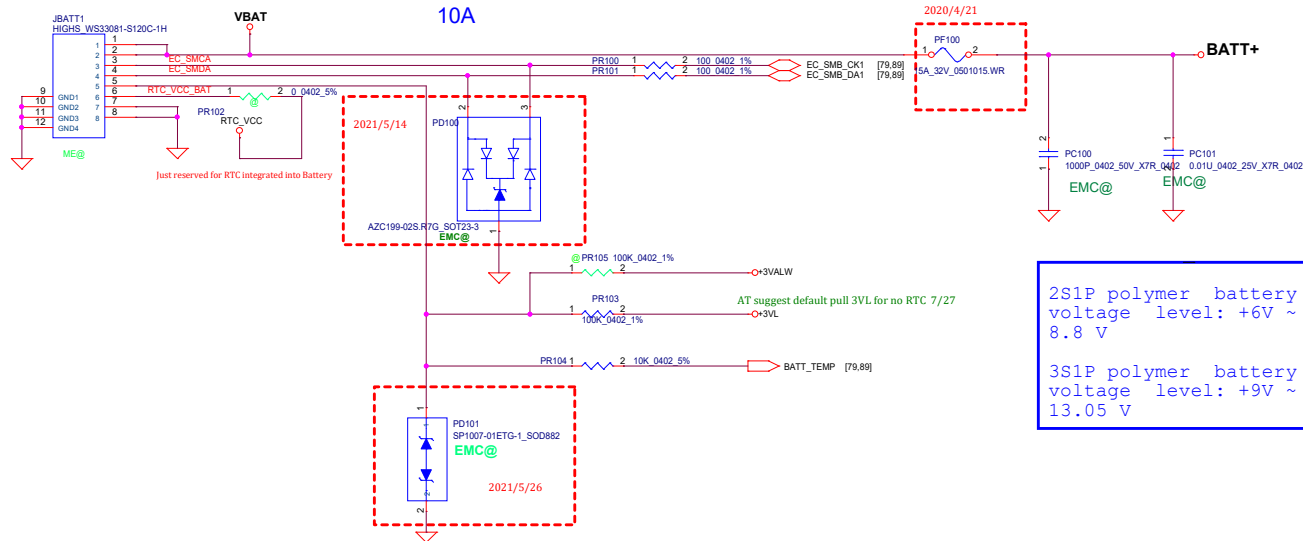


Hole



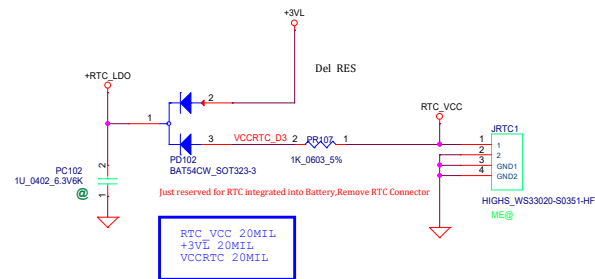
Shielding





2S1P polymer battery  
voltage level: +6V ~  
8.8 V

3S1P polymer battery  
voltage level: +9V ~  
13.05 V



5

4

3

2

1


D

C

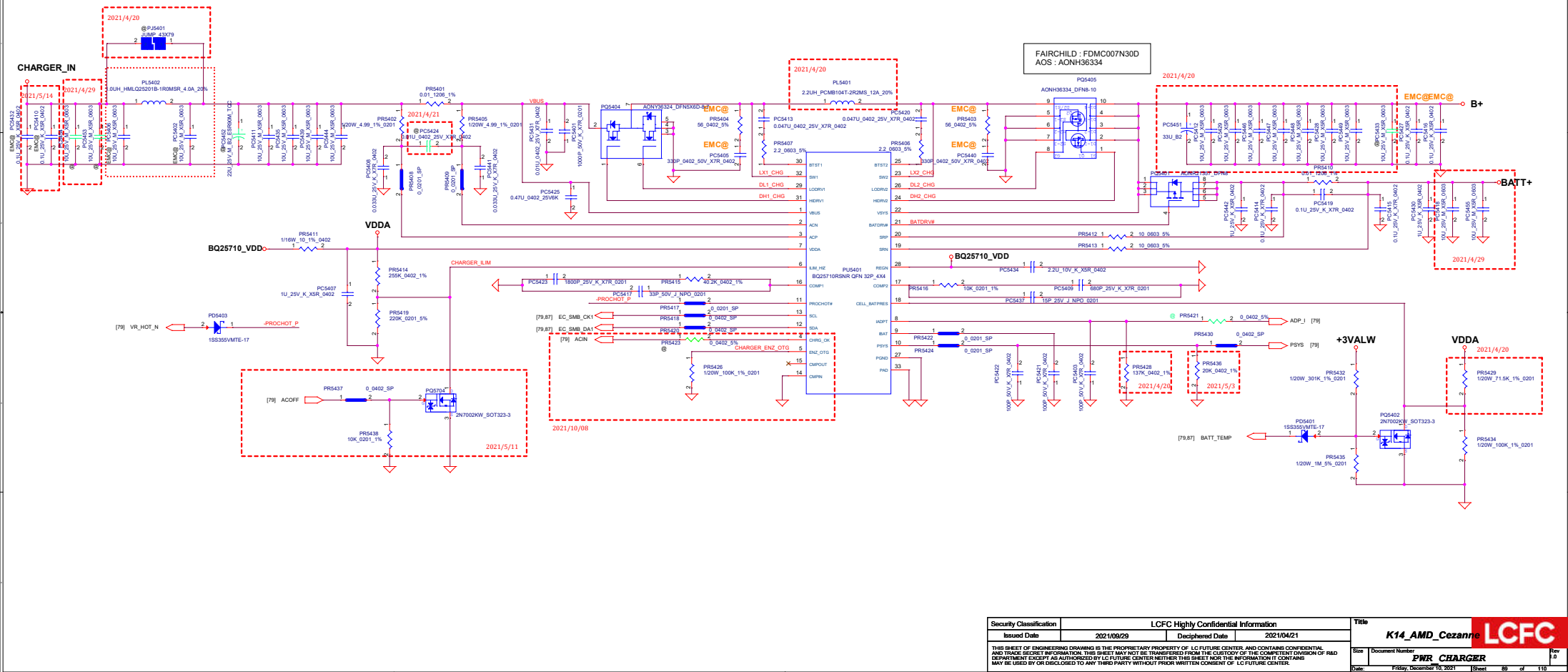
B

A

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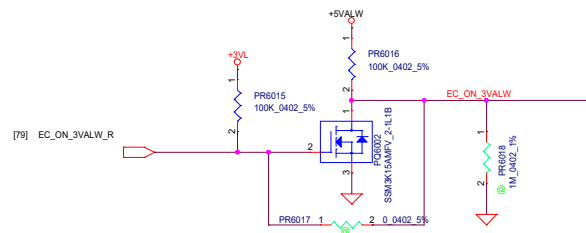
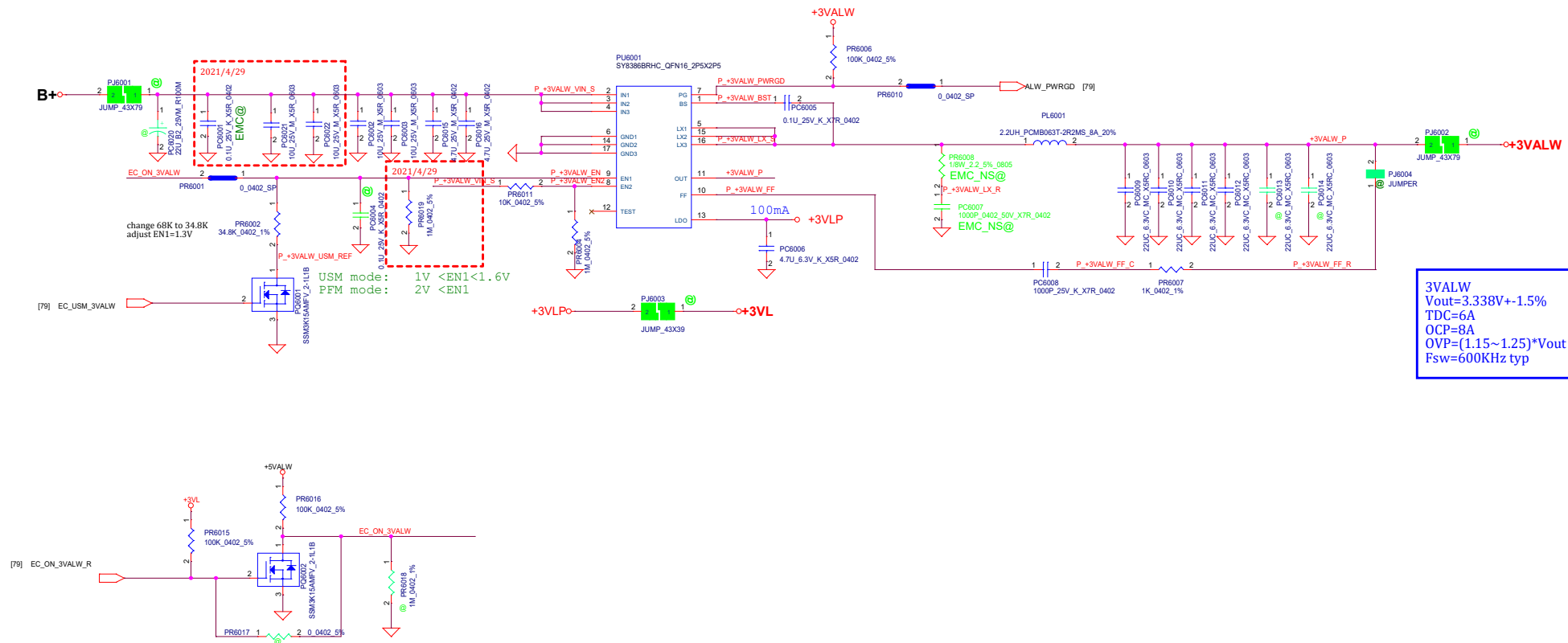




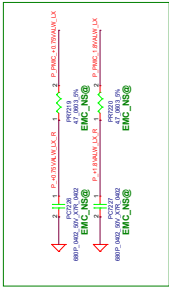


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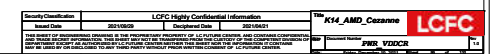


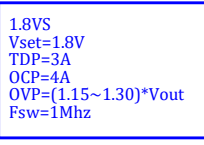





**LCFC**








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